TE0817 TRM

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Table of contents

Overview

The Trenz Electronic TE0817 is an industrial grade MPSoC SoM integrating an AMD Zynq UltraScale+ MPSoC, DDR4 SDRAM with 64-Bit width data bus connection, SPI Boot Flash memory for configuration and operation, transceivers and powerful switch-mode power supplies for all on-board voltages. A large number of configurable I/Os is provided via rugged high-speed stacking connections in a compact 5.2 cm x 7.6 cm form factor.

Refer to http://trenz.org/te0817-info for the current online version of this manual and other available documentation.

Key Features

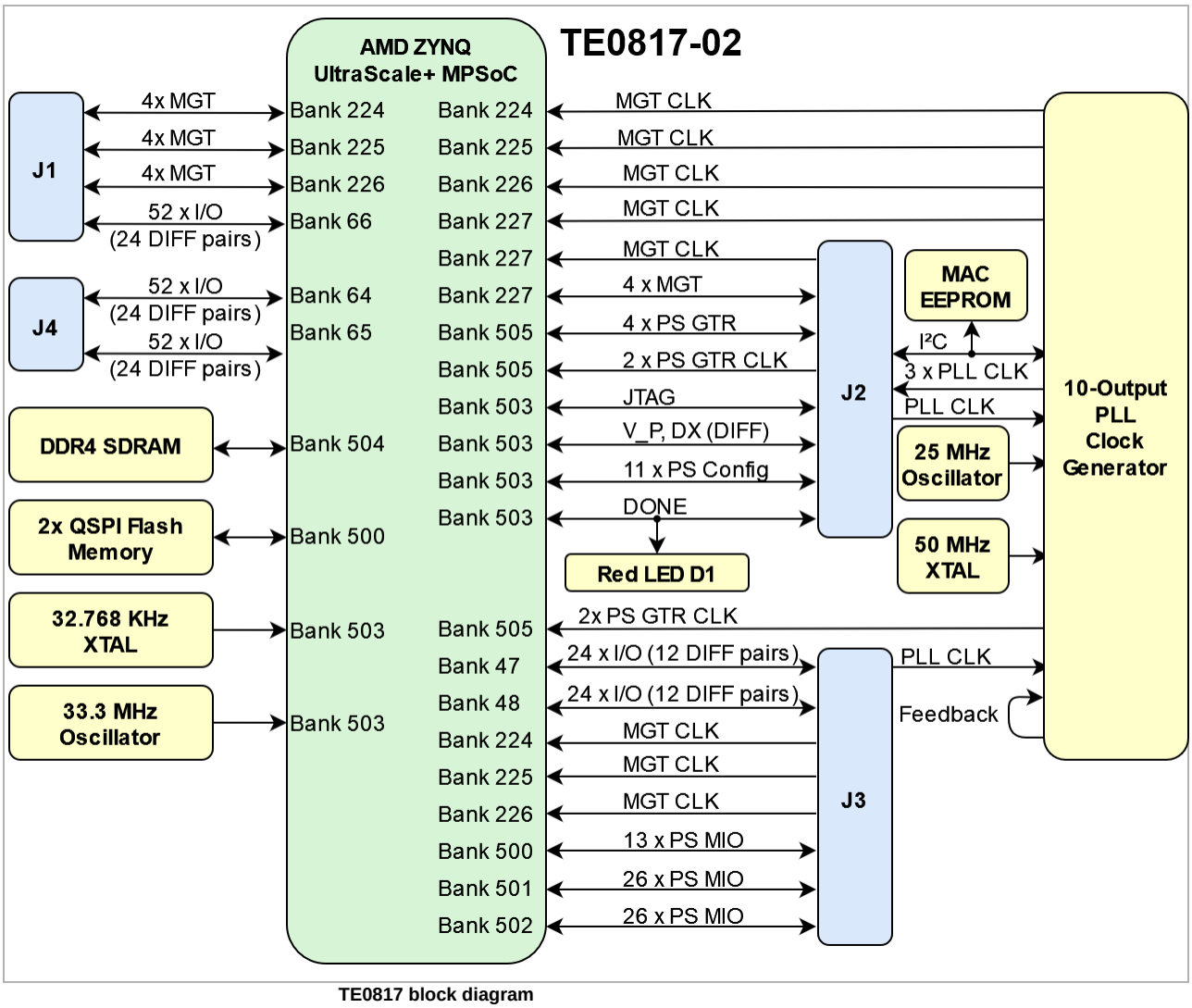
- **SoC**
  - Device: ZU4 / ZU5 / ZU7 [1)]
  - Engine: CG / EG / EV [1)]
  - Speedgrade: -1 / -2 / -3 [1)]
  - Temperature Range: Extended / Industrial [1)]
  - Package: FBVB900
- **RAM/Storage**
  - 4 GByte DDR4 SDRAM [2)]
  - 2 x 64 MByte Serial Flash
  - EEPROM with MAC address
- **On Board**
  - Oscillator
- **Interface**
  - 4 x B2B Connector (ADM6)
    - up to 204 PL IO
      - HP: 156
      - HD: 48
    - up to 65 PS MIO
    - 4 GTR
    - 16 GTH
    - I2C, JTAG
- **Power**
  - Power supply via B2B Connector needed.
- **Dimension**
  - 76 mm x 52 mm
- **Notes**

[1)] Please, take care of the possible assembly options. Furthermore, check whether the power supply is powerful enough for your FPGA design.

[2)] Up to 8 GByte are possible with a maximum bandwidth of 2400 MBit/s.

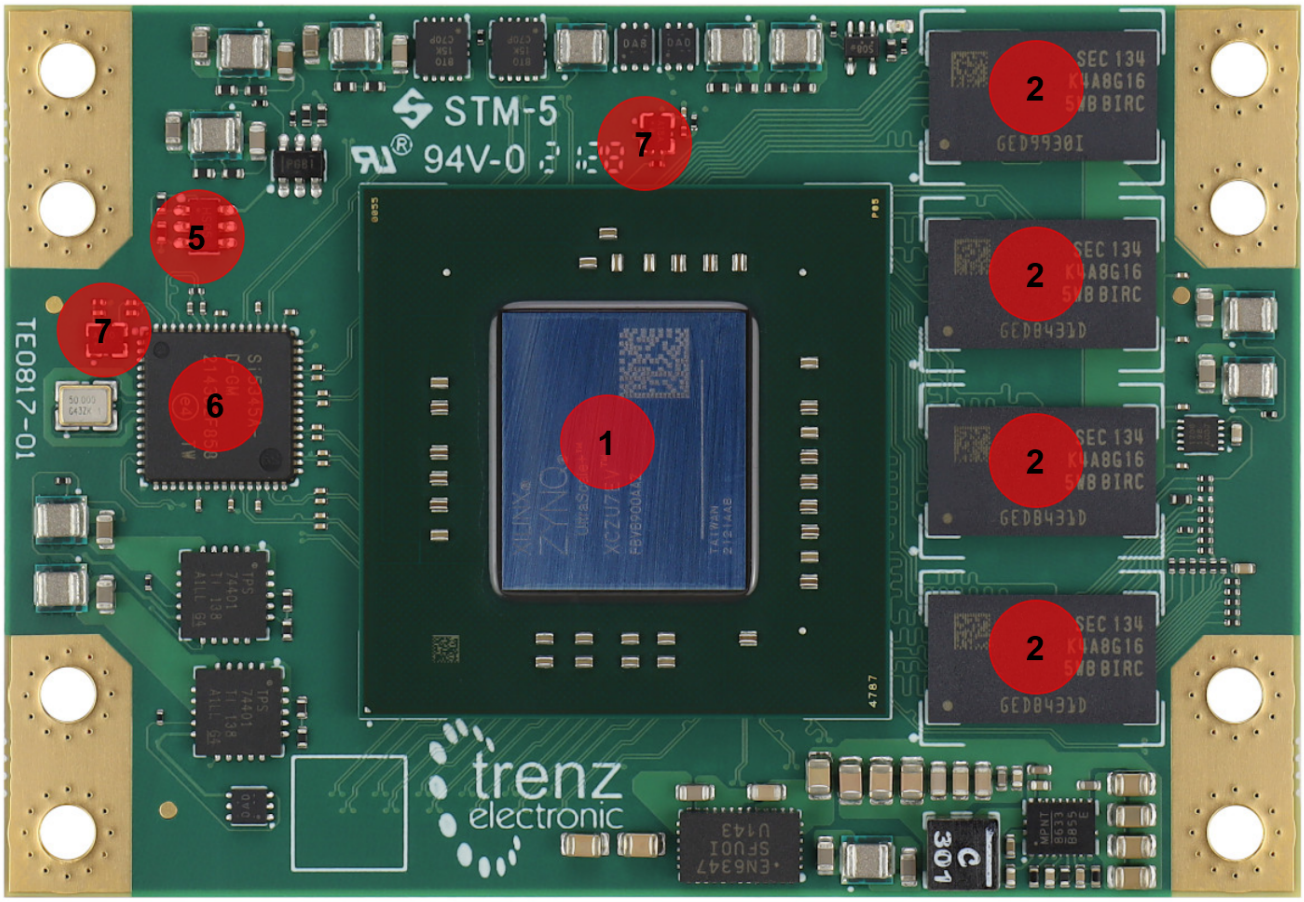
[3)] Please, take care of the possible assembly options.

Block Diagram



TE0817 block diagram

Main Components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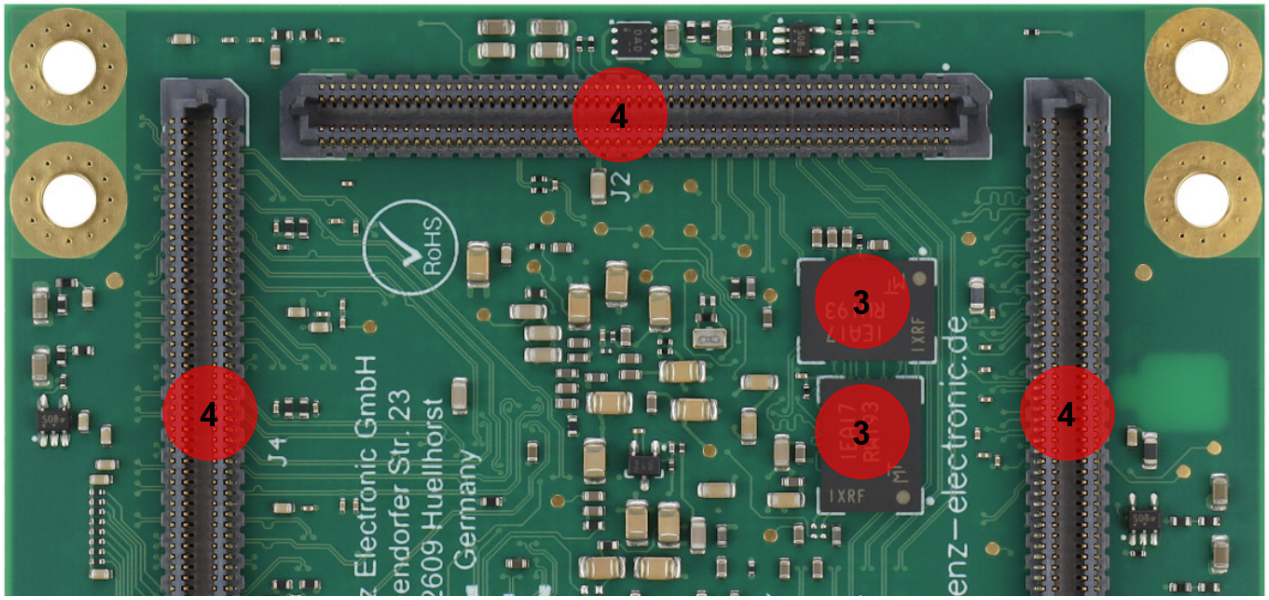
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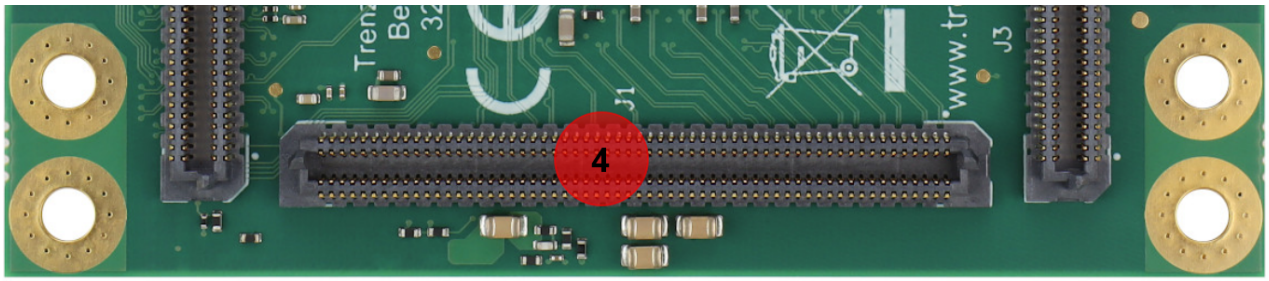
2609 Huellhorst
Germany
enz-electronic.de



TE0817 main components

1. SoC, U1
2. DDR4, U2, U3, U9, U12
3. Quad SPI Flash, U7, U17
4. Connector, J1, J2, J3, J4
5. EEPROM, U11
6. Clock Generator, U5
7. Oscillator, U25, U32

Initial Delivery State

Storage device name	Content	Notes
DDR4 SDRAM	not programmed	
Quad SPI Flash	not programmed	
EEPROM	not programmed besides factory programmed MAC address	
Programmable Clock Generator	not programmed	

Initial delivery state of programmable devices on the module

Signals, Interfaces and Pins

Connectors

Connector Type	Designator	Interface	IO CNT [1)]	Notes
B2B	J1	MGT PL	12 x MGT (RX /TX)	
B2B	J1	HP	52 SE / 24 DIFF	
B2B	J2	MGT PS	2 x MGT CLK	
B2B	J2	CLK	DIFF CLK	
B2B	J2	MGT PL	4 x MGT (RX /TX)	
B2B	J2	MGT PS	4 x MGT (RX /TX)	
B2B	J2	CFG	JTAG	
B2B	J2	CFG	MODE	
B2B	J3	HD	48 SE / 24 DIFF	

B2B	J3	MGT PL	3 x MGT CLK	
B2B	J3	CLK	DIFF CLK	
B2B	J3	MIO	65 GPIO	
B2B	J4	HP	104 SE / 48 DIFF	

[1] IO CNT depends on assembly variant. E.g. the MGTs are not available for all FPGAs

Board Connectors

Test Points

Test Point [1]	Signal	Notes [2]
TP1	PLL_SCL	pulled-up to SI_PLL_1V8
TP2	PLL_SDA	pulled-up to SI_PLL_1V8
TP3	DDR4-TEN	pulled-down to GND
TP4	VTT	
TP5	GND	
TP6	TCK	
TP7	TDI	
TP8	TDO	
TP9	TMS	
TP10	LP_0V85	
TP11	FP_0V85	
TP12	PL_VCCINT	
TP13	PS_PLL	
TP14	PS_GT_1V0	
TP15	FP_0V85	
TP16	DDR_2V5	
TP17	DCDC_2V0	
TP18	DDR_PLL	
TP19	PS_GT_1V0	
TP20	PL_VCU	
TP21	PS_AUX	
TP22	PS_AVCC	
TP23	VTT	
TP24	AUX_R	

TP25	AVTT_R	
TP26	AVCC_R	
TP27	PS_PLL	
TP28	PS_AVTT	
TP29	PS_AUX	
TP30	PS_AVCC	
TP31	LP_0V85	
TP32	GND	
TP33	PS_AVTT	
TP34	DDR_PLL	
TP35	DDR_2V5	
TP36	VREFA	
TP37	VREFA	
TP38	3.3VIN	
TP39	LP_DCDC	
TP40	PL_VCCINT	
TP41	DCDCIN	
TP42	DCDC_2V0	
TP43	PL_DCIN	
TP44	PL_GT_1V45	
TP45	PL_GT_1V45	
TP46	GT_DCDC	
TP47	PL_GT_1V15	
TP48	PL_GT_1V15	
TP49	PLL_3V3	
TP50	AUX_R	
TP51	PSBATT	
TP52	AVCC_R	
TP53	AVTT_R	
TP54	VCCO_47	
TP55	PL_VCU	
TP56	VCCO_48	
TP57	1V8_REFIN	
TP58	1V8_REFIN	
TP59	VCCO_64	

TP60	1V25_REF	
TP61	1V25_REF	
TP62	VCCO_65	
TP63	VCCO_66	
TP64	PLL_VDDA	
TP65	PLL_VDDA	
TP66	PLL_VDD	
TP67	PLL_VDD	
TP68	PS_1V8	
TP69	PL_1V8	
TP70	SI_PLL_1V8	
TP71	SI_PLL_1V8	
TP72	DDR4_1V2	

[1] Test points depend on revision: Not all testpoints are available for all revisions.

[2] Direction:

- IN: Input from the point of view of this board.
- OUT: Output from the point of view of this board.

Test Points Information

On-board Peripherals

Chip/Interface	Designator	Connected To	Notes
DDR4 SDRAM	U2, U3, U9, U12	SoC - PS	
Quad SPI Flash	U7, U17	SoC - PS	Booting.
EEPROM	U11	B2B - J2	
Clock Generator	U5	SoC, B2B	
Oscillator	U25	Clock Generator	25 MHz
Oscillator	U32	SoC	33.333333 MHz

On board peripherals

Configuration and System Control Signals

Connector+Pin	Signal Name	Direction[1)]	Description
J1.A45	POR_OVERRIDE	IN	Override power-on reset delay [2)].
J2.A30	PG_PLL_1V8	OUT	SI_PLL_1V8 power rail powered-up.
J2.A31	ERR_OUT	OUT	PS error indication [2)].
J2.A34	ERR_STATUS	OUT	PS error status [2)].
J2.A35	LP_GOOD	OUT	Low-power domain powered-up. Pulled up to 3.3VIN.
J2.A36	PLL_SCL	IN	I2C clock
J2.A37	PLL_SDA	IN/OUT	I2C data
J2.A40	PG_VCU	OUT	VCU power rail powered-up.
J2.A41	EN_PSGT	IN	Enable GTR transceiver power-up.
J2.A44 / J2.A45 / J2.A46 / J2.A47	TCK / TDI / TDO / TMS	Signal-dependent	JTAG configuration and debugging interface. JTAG reference voltage: PS_1V8
J2.B29	PG_PSGT	OUT	GTR transceivers powered-up.
J2.B30	PROG_B	IN/OUT	Power-on reset [2)]. Pulled-up to PS_1V8.
J2.B33	SRST_B	IN	System reset [2)]. Pulled-up to PS_1V8.
J2.B34	INIT_B	IN/OUT	Initialization completion indicator after POR [2)]. Pulled-up to PS_1V8.
J2.B37	PG_PL	OUT	Programmable logic powered-up.
J2.B38	EN_FPD	IN	Enable full-power domain power-up.
J2.B41	PG_FPD	OUT	Full-power domain powered-up.
J2.B42	EN_LPD	IN	Enable low-power domain power-up.
J2.B45	PG_DDR	OUT	DDR power supply powered-up.
J2.B46	DONE	OUT	PS done signal [2)]. Pulled-up to PS_1V8.
J2.B47	EN_DDR	IN	Enable DDR power-up.
J2.C30	EN_GT_L	IN	Not connected.
J2.C31	MR	IN	Manual reset.
J2.C32	PLL_SEL0	IN	PLL clock selection.

J2.C33	PLL_RST	IN	PLL reset.
J2.C35	EN_PL	IN	Enable programable logic power-up.
J2.C36	EN_GT_R	IN	Enable GTH transceiver power-up.
J2.C37	PLL_FDEC	IN	PLL Frequency decrementation.
J2.C44 / J2.C45 / J2.C46 / J2.C47	MODE3..0	IN	Boot mode selection [2]: • JTAG • QUAD-SPI (32 Bit) • SD1 (2.0) • eMMC (1.8 V) • SD1 LS (3.0) Supported Modes depends also on used Carrier.
J2.D29	EN_PLL_PWR	IN	Enable PLL power supply.
J2.D30	PLL_FINC	IN	PLL Frequency incrementation.
J2.D31	PLL_LOLn	OUT	Loss of lock status.
J2.D32	PLL_SEL1	IN	PLL clock selection.
J2.D33	PG_GT_R	OUT	GTH Transceivers powered-up.
J2.D37	PSBATT	IN	PS RTC Battery supply voltage [2] [3].
J2.D38	PUDC_B	IN	Configuration pull-ups setting [2]. Pulled-up to PL_1V8.
J2.D45 / J2.D46	DX_P / DX_N	-	SoC temperatur sensing diode pins [2].

[1] Direction:

- IN: Input from the point of view of this board.
- OUT: Output from the point of view of this board.

[2] See UG1085 for additional information.

[3] See Recommended Operating Conditions.

Controller signal.

Power and Power-On Sequence

Power Rails

Power Rail Name/ Schematic Name	Connector.Pin	Direction[1]	Notes
VCCO_66	J1.A32 / J1.A33	IN	
VREF_66	J1.A41	IN	

3.3VIN	J1.A54 / J1.A55 / J1.B55 / J1.B56	IN	
PL_1V8	J1.C32 / J1.C33 / J1.D33 / J1.D34	OUT	
PL_DCIN	J1.C56 / J1.C57 / J1.C58 / J1.C59 / J1.C60 / J1. D56 / J1.D57 / J1.D58 / J1.D59 / J1.D60	IN	
LP_DCDC	J2.A50 / J2.A51 / J2.A52 / J2.B50 / J2.B51 / J2.B52 / J2.C50 / J2.C51 / J2.C52 / J2.D50 / J2.D51 / J2.D52	IN	
DCDCIN	J2.A57 / J2.A58 / J2.A59 / J2.A60 / J2.B57 / J2.B58 / J2.B59 / J2.B60 / J2.C57 / J2.C58 / J2.C59 / J2.C60 / J2.D57 / J2.D58 / J2. D59 / J2.D60 /	IN	
PS_BATT	J2.D37	IN	
DDR_1V2	J2.D47	OUT	
PS_1V8	J2.C34 / J2.D34 / J3.A56 / J3.B56 / J3.C56 / J3.D56	OUT	
PLL_3V3	J3.A55	IN	
GT_DCDC	J3.A59 / J3.A60 / J3.B59 / J3.B60 / J3.C59 / J3.C60 / J3.D59 / J3.D60 /	IN	
VCCO_48	J3.C7 / J3.C8 / J3.D8 / J3. D9	IN	
VCCO_47	J3.C19 / J3.C20 / J3.D20 / J3.D21	IN	
VCCO_64	J4.B21 / J4.B39	IN	
VREF_64	J4.B30	IN	
VCCO_65	J4.C21 / J4.C39	IN	
VREF_65	J4.C30	IN	

[1] Direction:

- IN: Input from the point of view of this board.
- OUT: Output from the point of view of this board.

Module power rails.

Recommended Power up Sequencing

The power up sequencing highly depends on the use case. In general, it should be possible to enable /disable the processing system (PS) / programmable logic (PL) independently. Furthermore, within the processing logic it should be possible to enable/disable only low-power domain and/or low-power and full-power domain. Additionally, usage of GTR for PS side and GTH for PL side should be possible. Because of this flexibility the needed parts of the following table needs to be selected individually. For detailed information take a look into schematics.

Sequence	Net name	Recommended Voltage Range	Pull-up/down	Description	Notes
0	-	-	-	Configuration signal setup.	See Configuration and System Control Signals.

1 [1]	PSBATT	1.2 V ... 1.5 V	-	Battery connection.	Battery Power Domain usage. When not used, tie to GND.
1	3.3VIN	3.3 V (± 5 %)	-	Management power supply.	Management module power supply. 0.5 A recommended.
GTH / GTR Transceiver clocking (Only necessary in cases where the PLL clock is used for GTH / GTH.):					
1 [1]	GT_DCDC	3.3 V (± 3 %) [2]		GTH transceiver power supply.	Main module power supply for GTH / GTY transceiver. 5 A recommended. Power consumption depends mainly on design and cooling solution.
1 [1]	EN_PLL_PWR	-	PD [3], GND	PLL power enable.	
1 [1]	PG_PLL_1V8	-	PU [3], 3.3 V	PLL power good status.	
2	Processing System (PS):			Procedure for PS starting.	
2.1	Low-power domain:			Bring-up for low-power domain PS.	
2.1.1	LP_DCDC	3.3 V (± 3 %) [2]	-	Low-power domain power supply.	Main module power supply for low-power domain. 5.5 A recommended. Power consumption depends mainly on design and cooling solution.
2.1.2	EN_LPD	-	PU [3], 3.3 V	Low-power domain power enable.	
2.1.3	LP_GOOD	-	PU [3], 3.3 V	Low-power domain power good status.	Module power-on sequencing for low-power domain finished.
2.2	Full-power domain:			Bring-up for full-power domain PS.	Full-power PS domain needs powered low-power PS domain.
2.2.1	DCDCIN	3.3 V (± 5 %) [2]		Full-power domainand GTR transceiver power supply.	Main module power supply for full-power domain. 7 A recommended. Power consumption depends mainly on design and cooling solution.
2.2.2	EN_FPD	3.3 V	-	Full-power domain power enable.	

2.2.3	PG_FPD	-	PU [3], 3.3 V	Full-power domain power good status.	Module power-on sequencing for full-power domain finished.
2.2.4	EN_DDR	3.3 V	-	DDR memory power enable.	
2.2.5	PG_DDR		PU [3], 3.3 V	DDR memory power good status.	Module power-on sequencing for DDR memory finished.
2.3	GTR Transceiver			Procedure for GTR transceiver starting.	PS transceiver usage needs powered PS (low- and full-power domain).
2.3.1	EN_PSGT	3.3 V	-	GTR transceiver power enable.	
2.3.2	PG_PSGT	-	PU [3], 3.3 V	GTR transceiver power good status.	Module power-on sequencing for GTR transceiver finished.
2	Programmable Logic (PL)			Procedure for PL starting.	PS and PL can be started independently.
2.1	PL_DCIN	3.3 V (± 5 %) [2] [4]	-	Programmable logic power supply.	Main module power supply for programmable logic. 12 A recommended. Power consumption depends mainly on design and cooling solution.
2.2	EN_PL	-	PU [3], 3.3 V	Programmable logic power enable.	
2.3	PG_PL	-	PU [3], 3.3 V	Programmable logic power good status.	Module power-on sequencing for programmable logic finished. Periphery and variable bank voltages can be enabled on carrier.
2.4	VCCO_47 / VCCO_48 / VCCO_64 / VCCO_65 / VCCO_66	[5]	-	Module bank voltages.	Enable bank voltages after PG_PL deassertion.
2.5	PG_VCU	-	PU [3], 3.3 V	VCU power good status.	
3	GTH / GTY Transceiver			Procedure for GTH / GTY transceiver starting.	PL transceiver usage needs powered PL and low-power PS domain.

3.1	GT_DCDC	3.3 V (± 3 %) [2]	-	GTH transceiver power supply.	Main module power supply for GTH transceiver. 5 A recommended. Power consumption depends mainly on design and cooling solution.
3.2	EN_GT_R	3.3 V	-	GTH / GTY transceiver power enable.	
3.3	PG_GT_R	-	PU [3], 3.3 V	GTH / GTY transceiver power good status.	

[1] (optional)

[2] Dependent on the assembly option a higher input voltage may be possible.

[3] (on module)

[4] This value depends highly on DCDC U4. Higher values may be possible with different DCDCs. For more information consult schematic and according datasheets.

[5] See DS925 for additional information.

Baseboard Design Hints

Board to Board Connectors

5.2 x 7.6 cm UltraSoM+ modules use four Samtec AcceleRate HD High-Density Slim Body Arrays on bottom side.

- 4x ADM6-60-01.5-L-4-2 (240 pins, 60 per row)
  - Mates with ADF6-60-03.5-L-4-2

5.2 x 7.6 cm UltraSoM+ carrier use four Samtec AcceleRate HD High-Density Slim Body Arrays on top side.

- 4x ADF6-60-03.5-L-4-2 (160-pins)
  - Mates with ADM6-60-01.5-L-4-2

Features

- Board-to-Board Connector 240-pins, 60 contacts per row
- 0.025" (0.635 mm) pitch
- Data Rate: max 56 Gbps
- Mates with: ADM6/APF6
- Insulator Material: LCP, Black
- Contact Material: Copper Alloy
- Plating: Au or Sn over 50 µ" (1.27 µm) N
- Operating Temperature Range: -55 ºC to +125 ºC
- PCIe 5.0 capable: Yes
- Lead-Free Solderable: Yes
- RoHS Compliant: Yes

Connector Stacking height

When using the standard type on baseboard and module, the mating height is 5 mm.

Other mating heights are possible by using connectors with a different height:

Order number	REF number	Samtec Number	Type	Contribution to stacking height	Comment
30095	REF-30095	ADM6-60-01.5-L-4-2	Module connector	1.5 mm	Standard connector used on modules
31137	REF-31137	ADF6-60-03.5-L-4-2	Baseboard connector	3.5 mm	Standard connector used on carrier

Connectors.

Connector Speed Ratings

The AcceleRate HD High-Density connector speed rating depends on the stacking height; please see the following table:

Stacking height	Speed rating
5 mm	56 Gbps

Speed rating.

Current Rating

Current rating of Samtec AcceleRate HD High-Density B2B connectors is 1.34 A per pin (4 pins powered)

Connector Mechanical Ratings

- Shock: 100G, 6 ms Sine
- Vibration: 7.5G random, 2 hours per axis, 3 axes total

Manufacturer Documentation

File	Modified
PDF File 20200225_hsc_adm6-xx-01p5-xxx-4-a_adf6-xx-03p5-xxx-4-a.pdf	10 01, 2022 by Martin Rohrmüller
PDF File adf6.pdf	10 01, 2022 by Martin Rohrmüller
PDF File ADF6-XXX-XX.X-XXX-X-X-X-FOOTPRINT.PDF	10 01, 2022 by Martin Rohrmüller
PDF File adf6-xxx-xx.x-xxx-x-x-x-xr-mkt.pdf	10 01, 2022 by Martin Rohrmüller
PDF File adx6 mated document.pdf	10 01, 2022 by Martin Rohrmüller

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Technical Specifications

Absolute Maximum Ratings *)

Power Rail Name/ Schematic Name	Description	Min	Max	Unit
LP_DCDC	Micromodule Power	-0.300	6.0	V
DCDCIN	Micromodule Power	-0.300	7.0	V
GT_DCDC	Micromodule Power	-0.300	6.0	V
PL_DCIN 1)	Micromodule Power	-0.300	7.0	V
3.3VIN	Micromodule Power	-0.300	3.600	V
PLL_3V3	PLL power supply	-0.500	3.8	V
PS_BATT	RTC / BBRAM	-0.500	2.000	V
VCCO_47	HD IO Bank power supply	-0.500	3.400	V
VCCO_48	HD IO Bank power supply	-0.500	3.400	V
VCCO_64	HP IO Bank power supply	-0.500	2.000	V
VCCO_65	HP IO Bank power supply	-0.500	2.000	V
VCCO_66	HP IO Bank power supply	-0.500	2.000	V
VREF_64	Bank input reference voltage	-0.500	2.000	V
VREF_65	Bank input reference voltage	-0.500	2.000	V
VREF_66	Bank input reference voltage	-0.500	2.000	V

1) For REV01 use max. 4 V instead which depends highly on DCDC U4. Higher values are possible with different DCDCs. For more information consult schematic and according datasheets.

PS absolute maximum ratings

*) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Condition. Exposure to absolute-maximum rated conditions for extended periods may affect device reliability.

Recommended Operating Conditions

This TRM is generic for all variants. Temperature range can be different depending on assembly version. Voltage range is mostly the same during variants (exceptions are possible, depending on custom request)

Operating temperature range depends also on customer design and cooling solution. Please contact us for options.

- Variants of modules are described here: Article Number Information
- Modules with commercial temperature grade are equipped with components that cover at least the range of 0°C to 75°C
- Modules with extended temperature grade are equipped with components that cover at least the range of 0°C to 85°C
- Modules with industrial temperature grade are equipped with components that cover at least the range of -40°C to 85°C
- The actual operating temperature range will depend on the FPGA / SoC design / usage and cooling and other variables.

Parameter	Min	Max	Units	Reference Document
LP_DCDC [1)]	3.201	3.399	V	
DCDCIN [1)]	3.135	3.465	V	
GT_DCDC [1)]	3.201	3.399	V	
PL_DCIN [1) 2)]	3.135	3.465	V	
3.3VIN	3.135	3.465	V	
PLL_3V3	3.135	3.465	V	
PS_BATT	1.2	1.5	V	See FPGA datasheet.
VCCO_47	1.164	3.399	V	See FPGA datasheet.
VCCO_48	1.164	3.399	V	See FPGA datasheet.
VCCO_64	0.97	1.854	V	See FPGA datasheet.
VCCO_65	0.97	1.854	V	See FPGA datasheet.
VCCO_66	0.97	1.854	V	See FPGA datasheet.
VREF_64	0.6	1.2	V	See FPGA datasheet.
VREF_65	0.6	1.2	V	See FPGA datasheet.
VREF_66	0.6	1.2	V	See FPGA datasheet.

[1)] Dependent on the assembly option a higher input voltage may be possible.

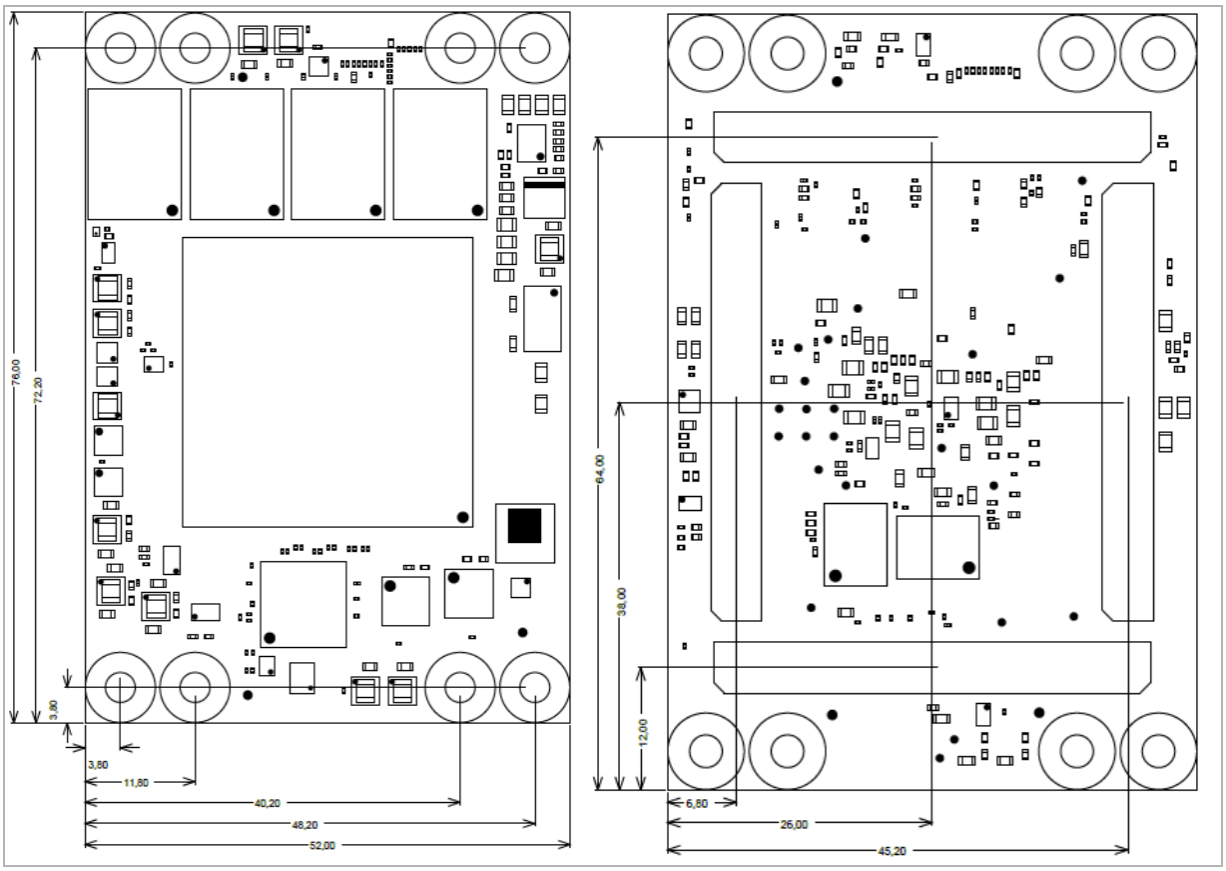
[2)] This value depends highly on REV01 DCDC U4. Higher values may possible with different DCDCs or different revision. For more information consult schematic and according datasheets.

Recommended operating conditions.

Physical Dimensions

- Module size: 76 mm × 52 mm. Please download the assembly diagram for exact numbers.
- Mating height with standard connectors: 5 mm.

PCB thickness: 1.74 mm (± 10 %).



Physical Dimension

Currently Offered Variants

Trenz shop TE0817 overview page	
English page	German page

Trenz Electronic Shop Overview

Revision History

Hardware Revision History

Board hardware revision number.

Date	Revision	Changes	Documentation Link

2024-04	REV02	1. Changed DCDC (U13) from EN6347QI to MPM3860GQW-Z and apdated according circuit. 2. Connected DDR4-TEN signals together for U2, U3, U9, and U12 and pulled them low via 499 Ohm resistor R127. Added testpoint TP3 for signal DDR4-TEN. 3. Changed voltage rail from 1.35 V to 1.45 V via adaption voltage divider resistor R30 and changed voltage rail name PL_GT_1V35 to PL_GT_1V45. 4. Changed voltage rail from 1.05 V to 1.15 V via adaption voltage divider resistors R33 and R35 and changed voltage rail name PL_GT_1V05 to PL_GT_1V15. 5. Added diode D2 between U41 pin 3 net MR and voltage rail 3.3VIN. 6. Added capacitors C202 ... C205 for VTT voltage rail VTT. 7. Added resistors R124 (default: not fitted) and R125 to supply U4 VCC either from PL_DCIN or from 3.3 VIN. 8. Changed resistor R76 from 4.22 kOhm to 9.09 kOhm to set current limit to nearly 14.3 A for U4. 9. Changed inductor (L9) from XGL4030-301MEC to XGL5030-351MEC. 10. Added remote sense option (default: not fitted): a. R126 for U30. b. R128 for U29. c. R129 for U31.	REV02

11. Added decoupling capacitors:
    a. C208 for U4.
    b. C211, C212, and C213 for U6.
    c. C216 for U10.
    d. C214 for U26.
    e. C215 for U27.
    f. C210 for U34.
    g. C196 for U39.
    h. C197 for U40.
    i. C198 for U42.
    j. C199 for U41.
    k. C200 for U44.
    l. C201, C206, and C207 for U1.
12. Added pull-up resistors for HOLD (R130) and WP (R131) signals for Flash U7.
13. Added pull-up resistors for HOLD (R132) and WP (R133) signals for Flash U17.
14. Changed capacitor (C132) from 1 nF, X7R to 1.2 nF, NP0.
15. Changed 10 nF capacitor (C112) from 16 V, 0402 to 10 V, 0201.
16. Changed 100 nF capacitors (C37, C95, C96, C130, and C131) from 6.3 V, X5R, 0201 to 50 V, X7R, 0402.
17. Changed capacitor (C76, C77, C134, C195) from 1 µF, 16 V to 2.2 µF, 10 V.
18. Changed capacitor (C129, C140, C141, C142, C143, C144, C145, C146, C147, C148, C153) from 10 µF, 16 V to 22 µF, 10 V.
19. Changed 22 uF capacitor (C70, C73, C74, C75) from 0805 to 0603.
20. Changed 22 uF capacitor (C78, C80, C81, C82, C83, C84, C85, C86, C87, C110, C152, C154, C178) from 6.3 V to 10 V.
21. Changed 100 Ohm resistors (R7, R10) from 0201, 0.05 W to 0402, 0.063 W.
22. Changed resistor R77 from 12 kOhm to 10 kOhm.
23. Changed resistors R41 and R58 from 2 kOhm to 2.49 kOhm.

		24. Added testpoints TP4, TP10, TP11, TP13, TP14, TP19, TP21, TP22, TP33 ... TP72. 25. Added UKCA logo. 26. Updated from library. 27. Changed signal trace length. 28. Updated documentation.	
-	REV01	First Production Release	REV01

Hardware Revision History

Hardware revision number can be found on the PCB board together with the module model number separated by the dash.

Document Change History

Date	Revision	Contributor	Description
Error rendering macro 'page-info' Ambiguous method overloading for method jdk.proxy279.$Proxy4022#hasContentLevelPermission. Cannot resolve which	**Error rendering macro 'page-info'** Ambiguous method overloading for method jdk.proxy279.$Proxy4022#hasContentLevelPermission. Cannot resolve which	**Error rendering macro 'page-info'** Ambiguous method overloading for method jdk.proxy279.$Proxy4022#hasContentLevelPermission. Cannot resolve which	• Updated to board REV02.

method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.

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confluence.core.ContentEntityObject][interface com.atlassian.user.User,class java.lang.String,class com.atlassian.confluence.core.ContentEntityObject]	confluence.core.ContentEntityObject][interface com.atlassian.user.User,class java.lang.String,class com.atlassian.confluence.core.ContentEntityObject]	confluence.core.ContentEntityObject][interface com.atlassian.user.User,class java.lang.String,class com.atlassian.confluence.core.ContentEntityObject]	
2023-03-02	v.17	Martin Rohrmüller	• Corrected max possible DDR4 assembly option
2023-01-16	v.14	ED	• Fixed issue in absolute maximum ratings
2022-11-08	v.13	ED	• Initial Document
--	all		• --

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		atlassian . confluence.core. ContentEntityObject]	

Document change history.

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