

# TE0841 AVN-20220802 QSPI boot problem at very slow rise time of module input voltage

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<b>Company</b>	Trenz Electronic GmbH
<b>PCN Number</b>	AVN-20220802
<b>Title</b>	AVN-20220802 QSPI boot problem at slow rise time of module input voltage
<b>Subject</b>	
<b>Issue Date</b>	AVN-20220802

## Products Affected

This issue can happen on following Trenz Electronic SoMs with native FPGA:

Affected Product	Note	Note
TE0710	4x5 Series	issue fixed Revision 3 and newer with Diode between PROG_B and INT_B
TE0711	4x5 Series	issue fixed Revision 2 and newer with Diode between PROG_B and INT_B
TE0712	4x5 Series	issue fixed Revision 4 and newer with Diode between PROG_B and INT_B
TE0713	4x5 Series	issue fixed Revision 3 and newer with Diode between PROG_B and INT_B
TE0714	3x5 Series VCCIO_0 is not sourced by internal 1.8V	issue fixed Revision 4 and newer with Diode between PROG_B and INT_B
TE0741	4x5 Series	issue fixed Revision 5 and newer with Diode between PROG_B and INT_B
TE0841	4x5 Series	issue fixed Revision 3 and newer with Diode between PROG_B and INT_B

## Description:

On 4x5 Module power switch (TPS27082LDDCR) will forward 3.3VIN voltage to 3.3V power rail. The switch is enabled by the internal power good signal from DCDC which provides the internal core voltages. This complies with the Xilinx power up sequencing. INIT\_B Pin will be released with pullup on this 3.3V power rail which forces the FPGA together with PROGRAM\_B to boot from QSPI Flash (See UG470). However, a too slow increase of the 3.3VIN voltage can result in the internal voltages being generated, but the 3.3V voltage is not yet sufficient for the QSPI flash, but high enough that the FPGA tries to boot from QSPI flash. In this case QSPI flash access can fail.

The same can happen with TE0714 on VIN and 3.3V in case assembly version with VCCIO\_0=3.3V is used.

## Solution:

1. Use input voltage power regulator with ramp time no more than 40ms (see ds181 Table 7: Power Supply Ramp Time)
2. The "EN1" (power on) signal should turn on when VIN and 3.3VIN are stable and reach 90% of the target value.
3. Trenz Electronic will check on every module, if this issue can be prevented with PCB and/or CPLD firmware modification on next PCB revision update

## Contact Information

If you have any questions related to this PCN, please contact Trenz Electronics Technical Support at

- [forum.trenz-electronic.de](https://forum.trenz-electronic.de)
- [wiki.trenz-electronic.de](https://wiki.trenz-electronic.de)
- [support@trenz-electronic.de](mailto:support@trenz-electronic.de) (subject = AVN-20220802)
- phone
  - national calls: 05741 3200-0
  - international calls: 0049 5741 3200-0

## Disclaimer

Any projected dates in this PCN are based on the most current product information at the time this PCN is being issued, but they may change due to unforeseen circumstances. For the latest schedule and any other information, please contact your local Trenz Electronic sales office, technical support or local distributor.

This PCN follows JEDEC Standard J-STD-046.