TEG2000 Test Board

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Overview

Refer to http://trm.pro/teg2000-info for the current online version of this manual and other available documentation.

This page describes briefly how to generate the fpga configuration file (Bitstream/cfg file) from the blink-example and how to program the FPGA. For a more detailed description of the tools follow the Quick start section of colognechip_ug_1002.

Key Features

- USB(JTAG/UART)
- LED

Revision History

Date	Project Built	Authors	Description
2024-04-15	TEG2000-test-board-cc-toolchain-win-trenz_20240415.zip	Waldemar Hanemann	• initial release

Design Revision History

Release Notes and Know Issues

Issues	Description	Workaround	To be fixed version
No known issues	---	---	---

Known Issues

Requirements

Software

Software	Version	Note
Yosys	0.37 +39	needed for RTL synthesis
GateMate EasyConvert Place&Route	2024.02-001	needed for implementation
openFPGALoader	v. 0.11.0	needed for loading bitstream into FPGA

Software

Hardware

Design supports following modules:

Module Model	Board Part Short Name	PCB Revision Support	DDR	QSPI Flash	EMMC	Others	Notes
TEG2000-01-P001*	--	REV01	--	16MB	--		

*used as reference

Hardware Modules

Design supports following carriers:

Carrier Model	Notes
TE0703*	We only support TE0703 up until now.

*used as reference

Hardware Carrier

Content

Design Sources

Type	Location	Notes
Toolchain	<project folder>\bin	script-based tools for synthesis, implementation, bitfile generation and programming
fpga project	<project folder>\workspace\blink\log <project folder>\workspace\blink\net <project folder>\workspace\blink\sim <project folder>\workspace\blink\src	.bat scripts can be used for synthesis & implementation & programming

Design sources

Prebuilt

File	File-Extension	Description

Constraint-File	*.ccf	FPGA pin constraint for pin-location, naming, input-output setting etc.
Design source-files	*.v , *.vhd	hdl design files describing the fpga functional description and I /O signals
Config File	*.cfg	Config File Data for FPGA. Comments included.
BIT-File	*.bit	FPGA (PL Part) Configuration File

Prebuilt files (only on ZIP with prebuilt content)

Download

Reference Design is available on:

- TEG2000 "Test Board" Reference Design

It contains the **tools**, the example project **blink** and several other sample projects(those are not documented here).

Design Flow & Launch

1. After downloading the test design go into the directory <project folder>\workspace\blink\
2. On Windows you can now run the *.bat scripts.
3. Run synth.bat
4. Run impl.bat
5. Connect the Board (TEG2000 + TE0703 carrier) to power and USB, see Getting started.
6. Run flash.bat to program the on-board qspi flash
7. Press reset, the green LED D2 should be blinking

System Design

HDL Sources

The design source files exist in verilog and in vhdl.

blink.vhd

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;

entity blink is
        port (
                clk : in std_logic;
                rst : in std_logic;
                led : out std_logic
```

```
        );
end entity;

architecture rtl of blink is

        component CC_PLL is
        generic (
                REF_CLK         : string;  -- reference input in MHz
                OUT_CLK         : string;  -- pll output frequency in MHz
                PERF_MD         : string;  -- LOWPOWER, ECONOMY, SPEED
                LOW_JITTER      : integer; -- 0: disable, 1: enable low
jitter mode
                CI_FILTER_CONST : integer; -- optional CI filter constant
                CP_FILTER_CONST : integer  -- optional CP filter constant
        );
        port (
                CLK_REF             : in  std_logic;
                USR_CLK_REF         : in  std_logic;
                CLK_FEEDBACK        : in  std_logic;
                USR_LOCKED_STDY_RST : in  std_logic;
                USR_PLL_LOCKED_STDY : out std_logic;
                USR_PLL_LOCKED      : out std_logic;
                CLK0                : out std_logic;
                CLK90               : out std_logic;
                CLK180              : out std_logic;
                CLK270              : out std_logic;
                CLK_REF_OUT         : out std_logic
        );
        end component;

        signal clk0    : std_logic;
        signal counter : unsigned(26 downto 0);

begin
        socket_pll : CC_PLL
        generic map (
                REF_CLK         => "10.0",
                OUT_CLK         => "100.0",
                PERF_MD         => "ECONOMY",
                LOW_JITTER      => 1,
                CI_FILTER_CONST => 2,
                CP_FILTER_CONST => 4
        )
        port map (
                CLK_REF             => clk,
                USR_CLK_REF         => '0',
                CLK_FEEDBACK        => '0',
                USR_LOCKED_STDY_RST => '0',
                USR_PLL_LOCKED_STDY => open,
                USR_PLL_LOCKED      => open,
                CLK0                => clk0,
                CLK90               => open,
                CLK180              => open,
                CLK270              => open,
                CLK_REF_OUT         => open
        );

        process(clk0)
        begin
                if rising_edge(clk0) then
                        if rst = '0' then
```

```
                                counter <= (others => '0');
                        else
                                counter <= counter + 1;
                        end if;
                end if;
        end process;

        led <= counter(26);

end architecture;
```

Constraints

Basic module constraints

blink.ccf

```
## blink.ccf
#
# Date: 2022-10-21
#
# Format:
# <pin-direction> "<pin-name>" Loc = "<pin-location>" | <opt.-constraints>;
#
# Additional constraints can be appended using the pipe symbol.
# Files are read line by line. Text after the hash symbol is ignored.
#
# Available pin directions:
#
# Pin_in
#   defines an input pin
# Pin_out
#   defines an output pin
# Pin_inout
#   defines a bidirectional pin
#
# Available pin constraints:
#
# SCHMITT_TRIGGER={true,false}
#   enables or disables schmitt trigger (hysteresis) option
# PULLUP={true,false}
#   enables or disables I/O pullup resistor of nominal 50kOhm
# PULLDOWN={true,false}
#   enables or disables I/O pulldown resistor of nominal 50kOhm
# KEEPER={true,false}
#   enables or disables I/O keeper option
# SLEW={slow,fast}
#   sets slew rate to slow or fast
# DRIVE={3,6,9,12}
#   sets output drive strength to 3mA..12mA
# DELAY_OBF={0..15}
#   adds an additional delay of n * nominal 50ps to output signal
# DELAY_IBF={0..15}
#   adds an additional delay of n * nominal 50ps to input signal
# FF_IBF={true,false}
#   enables or disables placing of FF in input buffer, if possible
# FF_OBF={true,false}
#   enables or disables placing of FF in output buffer, if possible
# LVDS_BOOST={true,false}
#   enables increased LVDS output current of 6.4mA (default: 3.2mA)
# LVDS_TERM={true,false}
#   enables on-chip LVDS termination resistor of nominal 100Ohm, in output
mode only
#
# Global IO constraints can be set with the default_GPIO statement. It can
be
# overwritten by individual settings for specific GPIOs, e.g.:
#   default_GPIO | DRIVE=3; # sets all output strengths to 3mA, unless
overwritten
#

Pin_in   "clk"  Loc = "IO_SB_A8" | SCHMITT_TRIGGER=true;
Pin_in   "rst"  Loc = "IO_EB_B0"; # SW3
Pin_out  "led"  Loc = "IO_SB_B4"; # D1
```

Additional Software

No additional software is needed.

App. A: Change History and Legal Notices

Document Change History

To get content of older revision go to "Change History" of this page and select older document revision number.

Date	Document Revision	Authors	Description
Error rendering macro 'page-info' Ambiguous method overloading for method jdk.proxy279.$Proxy4022#hasContentLevelPermission. Cannot	**Error rendering macro 'page-info'** Ambiguous method overloading for method jdk.proxy279.$Proxy4022#hasContentLevelPermission. Cannot	**Error rendering macro 'page-info'** Ambiguous method overloading for method jdk.proxy279.$Proxy4022#hasContentLevelPermission. Cannot	• add download link to test board subfolder

resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.

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atlassian . confluence.core. ContentEntityObject] [interface com. atlassian.user. User, class java. lang. String, class com. atlassian . confluence.core. ContentEntityObject]	atlassian . confluence.core. ContentEntityObject] [interface com. atlassian.user. User, class java. lang. String, class com. atlassian . confluence.core. ContentEntityObject]	atlassian . confluence.core. ContentEntityObject] [interface com. atlassian.user. User, class java. lang. String, class com. atlassian . confluence.core. ContentEntityObject]	
2024-04-16	v.13	Waldemar Hanemann	• initial release blinky
--	all	**Error rendering macro 'page-info'** Ambiguous	--

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Document change history.

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