

# TE Board Part Files

Most of the TE modules are available in different assembly options. Assembly option with different FPGA/SOC devices or other DDR sizes need an own board part file. In some cases also a PCB revision changes or a special carrier module combination needs a separate board part.

It's recommended to use the board part files only for this Vivado Version, for which it has been provided. Depending on the Schema Version of the XML-Files and Xilinx IP definitions, it is possible to use them with other Vivado versions, see Xilinx ug895.

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## Naming Conventions and Version

This Naming Convention will be used for the most Vivado 2016.2 Board Part Files and newer one.

Board Part Files consists on a base folder, a version sub folder with three xml files and one picture:

- Every assembly option of a module/carrier series where FPGA-Typ (Size, Speed/Temperature Grade) is changed, gets a new base folder.
- Every other assembly option or PCB-revision change, which has affects on the reference design settings, gets a new version sub folder.

## Board Part Base Folder

Board Part Names of the base folder consists of max. three parts separated by underline character.

	Usage of the part of name	Example 1	Example 2	Example 3	Example 4
<b>Name of the PCB Series</b>	Always	TE0726	TE0745	TE0720	TE0711
<b>FPGA Size</b>	Optional		30		35
<b>FPGA Speed/Temperature Grade</b>	Optional			1C	2C

## Board Part Version Folder

Version folder Name consists on a major and minor number separated by a dot (<major>.<minor>, example 1.0) Different Version folder means:

<b>Major</b>	<ul style="list-style-type: none"><li>• Changes on assembly option, which has effects on the reference design, for example DDR Size</li><li>• Boart Part for special Carrier/Module combination</li></ul>
<b>Minor</b>	<ul style="list-style-type: none"><li>• Changes on PCB-Revision, which has effects on the reference design</li></ul>

Attention: Changes on the settings of the TE Board Part Files by itself are not under version control at the moment, like described in Xilinx ug895. XML file includes a comment header with the date of the last change of the selected file.

## Location

Board Part Files will be delivered with our Reference Designs on our [https://shop.trenz-electronic.de/Download/?path=Trenz\\_Electronic/<group>/<form factor>/<module\\_name>/Reference\\_Design/<vivado\\_version>/<design\\_name>](https://shop.trenz-electronic.de/Download/?path=Trenz_Electronic/<group>/<form factor>/<module_name>/Reference_Design/<vivado_version>/<design_name>).

Board Part Files are located in the sub folder <design\_name>/board\_files/ of the downloadable Reference Design. For detailed information of the zip-file folder structure see: [Project Delivery - Directory Structure](#).

This folder includes also a \*\_board\_files.csv file with a list of all available board parts. This list is only used by TE-Scripts.

## Select Correct Board Part Files



Since 2018.3 special "Module Selection Guide" is included into "\_create\_win\_setup.cmd" and "\_create\_linux\_setup.sh"

- **Execute** "\_create\_win\_setup.cmd" or "\_create\_linux\_setup.sh"
- **Select** "Module Selection Guide" (press "0" and Enter)
- **Follow instructions**

- Check `<design_name>/board_files/<board_series>_board_files.csv` for available board part of the reference design:
  - The table shows all available board parts, which are delivered with the reference design
  - "ID" Unique ID for every board file in the project delivery
  - "PROID" is the whole article name, latest reference design are available with all variants
  - "PARTNAME" is the FPGA device setting of Vivado for the assembly variant
  - "BOARDNAME" is the corresponding board part file, which is used, files location is in `./board_files/<basename>/<Xil file id>/"`
  - "SHORTNAME" is the name for the board part specific sub folders in the reference design
  - "ZYNQFLASHSTYP" is the setting to configure the Flash via SDK
  - "FPGAFLASHSTYP" is the setting to configure the Flash via Vivado (first part only), the second and third part are QSPI mode and memory size in MB
  - "PCB\_REV" is supported PCB Revision
  - "DDR\_SIZE" is DDR size if available
  - "FLASH\_SIZE" is Flash size if available
  - "EMMC\_SIZE" is eMMC size if available
  - "OTHERS" other HW notes
  - "NOTES" additional notes
  - "DESIGN" filter for the reference design usage

[illegible]

- Check your order number and/or TE shop page to get module information of your PCB:  
- <https://shop.trenz-electronic.de/en/Products/Trenz-Electronic/<device familie>/<TE module serie>>

Home **Products** Download Company Services Jobs News Distributors

Products > Trenz Electronic > TE08XX - Zynq UltraScale+ > TE0808 - Zynq UltraScale+

Select your board part file on `design_basic_settings.cmd/sh`:  
Use unique name from CSV list (see 1.)

- Unique names are ID or PRODID (in the most cases) or BOARDNAME or SHORTNAME
- Revision number of the PRODID is the last one, which was available on last board part update. If there is no special board part for older revisions, this will be backward compatible. Please verify this on Vivado, see 4.

See [Reference Design: Getting Started](#) for more details.

- Project Summary**

### Project Settings

Project name: test\_board  
 Project location: B:\JVN\cores\2016-4\design\TIE0720/test\_board\vivado  
 Product family: Zynq-7000  
 Project part: [ZYNQ-7 TIE0720\\_1.UF\\_SPART PCB: REV02\\_REV03 \[xc7z020dqe484-1\]](#)  
 Top module name: [xvs\\_virapper](#)  
 Target language: VHDL  
 Simulator language: Mxld

### Board Part

Display names: ZYNQ-7 TIE0720\_1.UF\_SPART PCB: REV02\_REV03 → Name and supported PCB revisions  
 Board part name: trenz.biz/xc7z020\_spart0-1.0 → Board name: trenz.biz:<base folder>:part0:<version folder>  
 Repository path: B:\JVN\cores\2016-4\design\TIE0720/test\_board/board\_files → Repository path of the used board part file  
 URL: <https://wiki.trenz-electronic.de/display/PD/TIE0720+-+XGpio?c=oe> → Trenz Electronic Wiki URL with detailed PCB description  
 Board overview: ZYNQ-7 TIE0720\_1.UF board (form factor 4x5 cm) with S1248 DIO3L, 10Gb Ethernet, Speed grade -1 and industrial temperature grade. Supported PCB Revisions: REV02, REV03. → Short PCB description and supported PCB revisions

Vivado FPGA part : <family><size><package><speed grade>

### Synthesis

Status: Not started  
 Messages: No errors or warnings  
 Part: xc7z020dqe484-1  
 Strategy: [Vivado Synthesis Defaults](#)

### Implementation

Status: Not started  
 Messages: No errors or warnings  
 Part: xc7z020dqe484-1  
 Strategy: [Vivado Implementation Defaults](#)  
 Incremental compile: [IsOn](#)

See [Vivado Board Part Installation](#) and [Project Delivery - QuickStart](#)