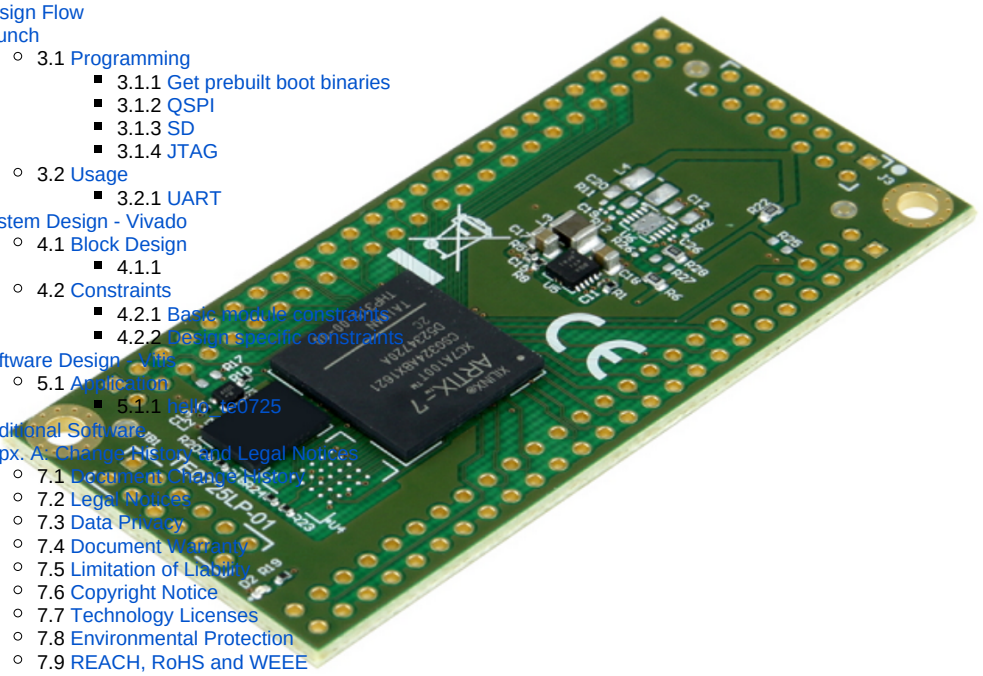
TE0725LP Test Board

Table of contents

Overview

- 1 Overview
  - 1.1 Key Features
  - 1.2 Revision History
  - 1.3 Release Notes and Know Issues
  - 1.4 Requirements
    - 1.4.1 Software
    - 1.4.2 Hardware
  - 1.5 Content
    - 1.5.1 Design Sources
    - 1.5.2 Additional Sources
    - 1.5.3 Prebuilt
    - 1.5.4 Download
- 2 Design Flow
- 3 Launch
  - 3.1 Programming
    - 3.1.1 Get prebuilt boot binaries
    - 3.1.2 QSPI
    - 3.1.3 SD
    - 3.1.4 JTAG
  - 3.2 Usage
    - 3.2.1 UART
- 4 System Design - Vivado
  - 4.1 Block Design
    - 4.1.1
  - 4.2 Constraints
    - 4.2.1 Basic module constraints
    - 4.2.2 Design specific constraints
- 5 Software Design - Vitis
  - 5.1 Application
    - 5.1.1 hello_te0725
- 6 Additional Software
- 7 Appx. A: Change History and Legal Notices
  - 7.1 Document Change History
  - 7.2 Legal Notices
  - 7.3 Data Privacy
  - 7.4 Document Warranty
  - 7.5 Limitation of Liability
  - 7.6 Copyright Notice
  - 7.7 Technology Licenses
  - 7.8 Environmental Protection
  - 7.9 REACH, RoHS and WEEE
- 8 Table of contents



MicroBlaze Design with Hello TE0725 example in endless loop.

Refer to http://trenz.org/te0725lp-info for the current online version of this manual and other available documentation.

Key Features

- Vitis/Vivado 2021.2
- MicroBlaze
- QSPI
- I2C
- UART

Revision History

Date	Vivado	Project Built	Authors	Description
2022-08-31	2021.2	TE0725LP-test_board_noprebuilt-vivado_2021.2-build_15_20220831152107.zip TE0725LP-test_board-vivado_2021.2-build_15_20220831152107.zip	Waldemar Hanemann	• 2021.2 update • Documentation style update
2020-04-20	2019.2	TE0725LP-test_board_noprebuilt-vivado_2019.2-build_10_20200420093012.zip TE0725LP-test_board-vivado_2019.2-build_10_20200420092959.zip	John Hartfiel	• 2019.2 update
2019-11-19	2018.2	TE0725LP-test_board_noprebuilt-vivado_2018.2-build_04_20191119080754.zip TE0725LP-test_board-vivado_2018.2-build_04_20191119080742.zip	John Hartfiel	• bugfix board part files clk settings
2018-08-16	2018.2	TE0725LP-test_board-vivado_2018.2-build_02_20180816093341.zip TE0725LP-test_board_noprebuilt-vivado_2018.2-build_02_20180816093354.zip	John Hartfiel	• 2018.2 update
2018-03-19	2017.4	TE0725LP-test_board-vivado_2017.4-build_07_20180319162005.zip TE0725LP-test_board_noprebuilt-vivado_2017.4-build_07_20180319162259.zip	John Hartfiel	• initial release

Design Revision History

Release Notes and Know Issues

Issues	Description	Workaround	To be fixed version
No known issues	---	---	---

Known Issues

Requirements

Software

Software	Version	Note
Vitis	2021.2	needed, Vivado is included into Vitis installation

Software

Hardware

Basic description of TE Board Part Files is available on TE Board Part Files.

Complete List is available on <design name>/board_files/*_board_files.csv

Design supports following modules:

Module Model	Board Part Short Name	PCB Revision Support	DDR	QSPI Flash	EMMC	Others	Notes
TE0725LP-01-100-2C	100	REV01	NA	32MB	NA	NA	3.3V Input Voltage
TE0725LP-01-100-2D	100	REV01	NA	32MB	NA	NA	1.8V Input Voltage
TE0725LP-01-100-2L	100	REV01	NA	32MB	NA	NA	1.8V Input Voltage
TE0725LP-01-100-2I	100_2i	REV01	NA	32MB	NA	NA	1.8V Input Voltage
TE0725LP-01-72C-1	100	REV01	NA	32MB	NA	NA	3.3V Input Voltage
TE0725LP-01-72C-1T	100	REV01	NA	32MB	NA	NA	1.8V Input Voltage
TE0725LP-01-72I-1T	100_2i	REV01	NA	32MB	NA	NA	1.8V Input Voltage
TE0725LP-01-72C-1U	100	REV01	NA	32MB	NA	NA	1.8V Input Voltage
TE0725LP-01-72C-1H	100	REV01	NA	32MB	NA	with hyperflash	3.3V Input Voltage

Hardware Modules

Design supports following carriers:

Carrier Model	Notes

Hardware Carrier

Additional HW Requirements:

Additional Hardware	Notes
TE0790 JTAG Programmer	Important: Depending on assembly version, it's not possible to supply module via TE0790. If it's possible, it's not recommended to use TE0790 for power supply(TE0790 TRM#PowerandPower-OnSequence)
External power supply	3.3V or 1.8V depending on assembly variant

Additional Hardware

Content

For general structure and of the reference design, see Project Delivery - AMD devices

Design Sources

Type	Location	Notes
Vivado	<design name>/block_design <design name>/constraints <design name>/ip_lib	Vivado Project will be generated by TE Scripts
Vitis	<design name>/sw_lib	Additional Software Template for Vitis and apps_list.csv with settings automatically for Vitis app generation

Design sources

Additional Sources

Type	Location	Notes
--	--	--

Additional design sources

Prebuilt

File	File-Extension	Description
BIT-File	*.bit	FPGA (PL Part) Configuration File
DebugProbes-File	*.ltx	Definition File for Vivado/Vivado Labtools Debugging Interface
Diverse Reports	---	Report files in different formats
Hardware-Platform-Specification-Files	*.xsa	Exported Vivado Hardware Specification for Vitis and PetaLinux
LabTools Project-File	*.lpr	Vivado Labtools Project File
MCS-File	*.mcs	Flash Configuration File with Boot-Image (MicroBlaze or FPGA part only)
MMI-File	*.mmi	File with BRAM-Location to generate MCS or BIT-File with *.elf content (MicroBlaze only)
Software-Application-File	*.elf	Software Application for Zynq or MicroBlaze Processor Systems

Prebuilt files (only on ZIP with prebult content)

Download

Reference Design is only usable with the specified Vivado/Vitis/PetaLinux version. Do never use different Versions of Xilinx Software for the same Project.

Reference Design is available on:

- TE0725LP "Test Board" Reference Design

Design Flow

Reference Design is available with and without prebuilt files. It's recommended to use TE prebuilt files for first lunch.

Trenz Electronic provides a tcl based built environment based on Xilinx Design Flow.

See also:

- AMD Development Tools#XilinxSoftware-BasicUserGuides
- Vivado Projects - TE Reference Design
- Project Delivery.

The Trenz Electronic FPGA Reference Designs are TCL-script based project. Command files for execution will be generated with "_create_win_setup.cmd" on Windows OS and "_create_linux_setup.sh" on Linux OS.

TE Scripts are only needed to generate the vivado project, all other additional steps are optional and can also executed by Xilinx Vivado/Vitis GUI. For currently Scripts limitations on Win and Linux OS see: Project Delivery Currently limitations of functionality

Caution! Win OS has a 260 character limit for path lengths which can affect the Vivado tools. To avoid this issue, use Virtual Drive or the shortest possible names and directory locations for the reference design (for example "x:\<project folder>")

1. Run _create_win_setup.cmd/_create_linux_setup.sh and follow instructions on shell:

_create_win_setup.cmd/_create_linux_setup.sh

```
-----------------------Set design paths--------------------------
-- Run Design with: _create_win_setup
-- Use Design Path: <absolute project path>
-----------------------------------------------------------------
-----------------------TE Reference
Design-------------------------
-----------------------------------------------------------------
-- (0)  Module selection guide, project creation...prebuilt export...
-- (1)  Create minimum setup of CMD-Files and exit Batch
-- (2)  Create maximum setup of CMD-Files and exit Batch
-- (3)  (internal only) Dev
-- (4)  (internal only) Prod
-- (c)  Go to CMD-File Generation (Manual setup)
-- (d)  Go to Documentation (Web Documentation)
-- (g)  Install Board Files from Xilinx Board Store (beta)
-- (a)  Start design with unsupported Vivado Version (beta)
-- (x)  Exit Batch (nothing is done!)
----
Select (ex.:'0' for module selection guide):
```

2. Press 0 and enter to start "Module Selection Guide"
3. Create project and follow instructions of the product selection guide, settings file will be configured automatically during this process.
    - optional for manual changes: Select correct device and Xilinx install path on "design_basic_settings.cmd" and create Vivado project with "vivado_create_project_guimode.cmd"

Note: Select correct one, see also Vivado Board Part Flow

a. Create hardware description file (.xsa file) for PetaLinux project and export to prebuilt folder

run on Vivado TCL (Script generates design and export files into "<project folder>\prebuilt\hardware\<short name>")

```
TE::hw_build_design -export_prebuilt
```

Using Vivado GUI is the same, except file export to prebuilt folder.

4. Generate Programming Files with Vitis

run on Vivado TCL (Script generates applications and bootable files, which are defined in "test_board\sw_lib\apps_list.csv")

```
TE::sw_run_vitis -all
TE::sw_run_vitis (optional; Start Vitis from Vivado GUI or start
with TE Scripts on Vivado TCL)
```

Note: Scripts generate applications and bootable files, which are defined in "sw_lib\apps_list.csv"

App from Firmware folder will be add into BlockRAM. If you add other app, you must select *.elf

manually on Vivado

TCL scripts generate also platform project, this must be done manually in case GUI is used. See Vitis

5. (optional) Copy Application (hello_te0725.elf) from prebuilt-folder into \firmware\microblaze_0\ and regenerate design with

run on Vivado TCL (Script generates design and export files into "<project folder>\prebuilt\hardware\<short name>")

```
TE::hw_build_design -export_prebuilt
```

Launch

Programming

Check Module and Carrier TRMs for proper HW configuration before you try any design.

Xilinx documentation for programming and debugging: Vivado/SDK/SDSoC-Xilinx Software Programming and Debugging

Get prebuilt boot binaries

1. Run _create_win_setup.cmd/_create_linux_setup.sh and follow instructions on shell
2. Press 0 and enter to start "Module Selection Guide"
    a. Select assembly version
    b. Validate selection
    c. Select create and open delivery binary folder

Note: Folder "<project folder>_binaries_<Article Name>" with subfolder "boot_<app name>" for different applications will be generated

QSPI

1. Connect JTAG and power on carrier with module
2. Open Vivado Project with "vivado_open_existing_project_guimode.cmd" or if not created, create with "vivado_create_project_guimode.cmd"

run on Vivado TCL (Script programs .mcs-File on QSPI flash)
`TE::pr_program_flash -swapp hello_te0725`

3. Press the reset button to start the application and see the output in the console

SD

Not used on this Example.

JTAG

1. Connect JTAG and power on PCB
2. Open Vivado HW Manager
3. Program FPGA with Bitfile from "prebuilt\hardware\<short dir>\"

Usage

1. Prepare HW like described on section Programming
2. Connect UART USB (most cases same as JTAG)
3. 1. FPGA Loads Bitfile from Flash

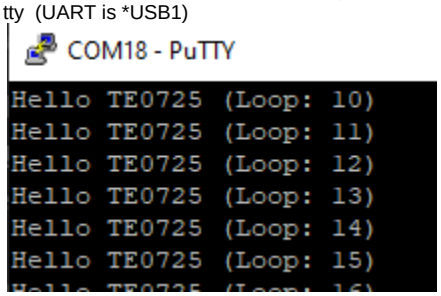
   3. Hello Trenz will be run on UART console.

   info: Do not reboot, if Bitfile programming over JTAG is used as programming method.

   a. ## UART

   Open Serial Console (e.g. putty) Hello TE0725 will run on endless loop.

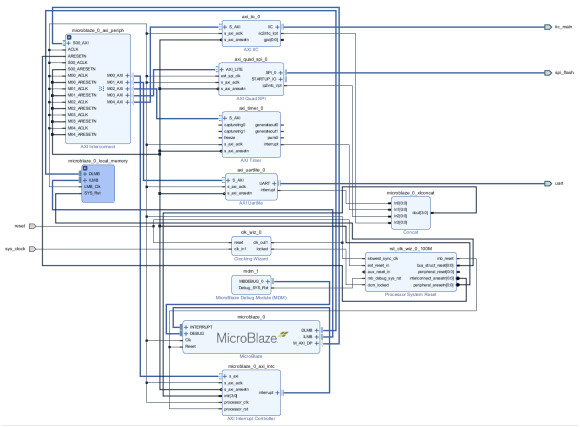
   i. Speed: 9600
   ii. COM Port: Win OS, see device manager, Linux OS see dmesg |grep tty (UART is *USB1)



Power On PCB (Do not restart, if you use Bitfile programming)

System Design - Vivado

Block Design



Constraints

Basic module constraints

_i_bitgen_common.xdc

```
set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design]
set_property BITSTREAM.CONFIG.CONFIGRATE 66 [current_design]
set_property CONFIG_VOLTAGE 1.8 [current_design]
set_property CFGBVS GND [current_design]
set_property BITSTREAM.CONFIG.SPI_32BIT_ADDR YES [current_design]
set_property BITSTREAM.CONFIG.SPI_BUSWIDTH 4 [current_design]
set_property BITSTREAM.CONFIG.M1PIN PULLNONE [current_design]
set_property BITSTREAM.CONFIG.M2PIN PULLNONE [current_design]
set_property BITSTREAM.CONFIG.M0PIN PULLNONE [current_design]

set_property BITSTREAM.CONFIG.USR_ACCESS TIMESTAMP [current_design]
```

Design specific constraints

Software Design - Vitis

For SDK project creation, follow instructions from:

Vitis

Application

Template location: "<project folder>\sw_lib\sw_apps\"

hello_te0725

Trenz Hello TE0725 example as endless loop. Output on console.

Template location: \sw_lib\sw_apps\hello_te0725

The printed Text can be modified.

Additional Software

No additional software is needed.

Appx. A: Change History and Legal Notices

Document Change History

To get content of older revision got to "Change History" of this page and select older document revision number.

Date	Document Revision	Authors	Description
Error rendering macro 'page-info' Ambiguous method overloading for method jdk.proxy279.$Proxy4022#hasContentLevelPe	**Error rendering macro 'page-info'** Ambiguous method overloading for method jdk.proxy279.$Proxy4022#hasContentLevelPe	**Error rendering macro 'page-info'** Ambiguous method overloading for method jdk.proxy279.$Proxy4022#hasContentLevelPe	• 2021.2 update • Documentation style update

rmission . Cannot resolve which method to invoke for [null, class java. lang. String, class com. atlassian . confluen ce. pages. Page] due to overlapp ing prototyp es between : [interfac e com. atlassian . confluen ce.user. Conflue nceUser , class java. lang.

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String, class com. atlassian . confluen ce.core. Content EntityOb ject] [interfac e com. atlassian .user. User, class java. lang. String, class com. atlassian . confluen ce.core. Content EntityOb ject]	String, class com. atlassian . confluen ce.core. Content EntityOb ject] [interfac e com. atlassian .user. User, class java. lang. String, class com. atlassian . confluen ce.core. Content EntityOb ject]	String, class com. atlassian . confluen ce.core. Content EntityOb ject] [interfac e com. atlassian .user. User, class java. lang. String, class com. atlassian . confluen ce.core. Content EntityOb ject]	
2020-04-20	v.9	John Hartfiel	• 2019.2 release • docu update
2019-11-19	v.8	John Hartfiel	• bugfix board part files
2018-08-16	v.6	John Hartfiel	• 2018.2 release
2018-06-05	v.5	John Hartfiel	• Typo correction UART Speed

2018-03-19	v.3	John Hartfiel	• 2017.4 release
	All	**Error rendering macro 'page-info'** Ambiguous method overloading for method jdk.proxy279.$Proxy4022#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian	

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Document change history.

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REACH, RoHS and WEEE

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Error rendering macro 'page-info'

Ambiguous method overloading for method jdk.proxy279.$Proxy4022#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]