TEC0850 MAX10 - SMB

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Overview

TEC0850 design for MAX10 FPGA U18: 10M08SAU169C8G.

Feature Summary

- SC to HD-IO Bank Interface
- I²C Backplane interface
- I²C System Control interface
- Power control
- Power status
- FAN Control
- FAN Status
- Power status indication

Firmware Revision and supported PCB Revision

See Document Change History.

Product Specification

Port Description

Name / opt. VHD Name	Direction	Pin	Bank Power	Description
ADBUS0	in	G9	3V_D	FTDI TCK
ADBUS1	in	F10	3V_D	FTDI TDI
ADBUS2	out	E10	3V_D	FTDI TDO
ADBUS3	in	D9	3V_D	FTDI TMS

AVDD_SHDN	inout	G10	3V_D	AVDD Shutdown / AVDD OV/UV
BCBUS0	-	D12	3V_D	FTDI (JTAG/UART, U4) / currently_not_used
BCBUS1	-	E13	3V_D	FTDI (JTAG/UART, U4) / currently_not_used
BCBUS2	-	E12	3V_D	FTDI (JTAG/UART, U4) / currently_not_used
BCBUS3	-	F13	3V_D	FTDI (JTAG/UART, U4) / currently_not_used
BCBUS4	-	F12	3V_D	FTDI (JTAG/UART, U4) / currently_not_used
BDBUS0 / FTDI_RXD	-	B11	3V_D	UART FTDI U4
BDBUS1 / FTDI_TXD	-	A12	3V_D	UART FTDI U4
BDBUS2	-	B12	3V_D	FTDI (JTAG/UART, U4) / currently_not_used
BDBUS3	-	C11	3V_D	FTDI (JTAG/UART, U4) / currently_not_used
BDBUS4	-	B13	3V_D	FTDI (JTAG/UART, U4) / currently_not_used
BDBUS5	-	C12	3V_D	FTDI (JTAG/UART, U4) / currently_not_used
BDBUS6	-	C13	3V_D	FTDI (JTAG/UART, U4) / currently_not_used
BDBUS7	-	D11	3V_D	FTDI (JTAG/UART, U4) / currently_not_used
CONF_DONE	-	C5	3V_D	/ currently_not_used
DET_BPR	-	H2	3V_D	/ currently_not_used
DET_RIO	-	H3	3V_D	/ currently_not_used
DONE	in	N3	PS_1V8	FPGA Done
EN_3V3	out	C10	3V_D	3.3V Power Enable
EN_DAC1	out	E6	3V_D	DAC1 Power Enable
EN_DAC2	out	E8	3V_D	DAC2 Power Enable
EN_DAC3	out	B6	3V_D	DAC3 Power Enable
EN_DAC4	out	A6	3V_D	DAC4 Power Enable
EN_DDR	out	G13	3V_D	DDR Power Enable
EN_FPD	out	L12	3V_D	FPD Power Enable
EN_LPD	out	J13	3V_D	LPD Power Enable
EN_PSGT	out	B9	3V_D	PSGT Power Enable
ERR_OUT	-	G5	PS_1V8	/ currently_not_used
ERR_STATUS	-	H6	PS_1V8	/ currently_not_used
F_TCK	out	N2	PS_1V8	FPGA TCK
F_TDI	out	M1	PS_1V8	FPGA TDI
F_TDO	in	K1	PS_1V8	FPGA TDO
F_TMS	out	J1	PS_1V8	FPGA TMS
F1PWM	out	H10	3V_D	FAN PWM Control
F1SENSE	in	J9	3V_D	FAN Sense
FTDI_RST	out	E9	3V_D	FTDI Reset
GA0	-	F8	3V_D	Backplane address / currently_not_used
GA0_R	-	F9	3V_D	Backplane address, pullup/down enable / currently_not_used
GA1	-	A2	3V_D	Backplane address/ currently_not_used
GA1_R	-	B2	3V_D	Backplane address, pullup/down enable / currently_not_used

GA2	-	A3	3V_D	Backplane address/ currently_not_used
GA2_R	-	B3	3V_D	Backplane address, pullup/down enable / currently_not_used
GA3	-	A4	3V_D	Backplane address/ currently_not_used
GA3_R	-	B4	3V_D	Backplane address, pullup/down enable / currently_not_used
IEEE_SW_NC	-	C9	3V_D	/ currently_not_used
IEEE_SW_NO	-	A11	3V_D	/ currently_not_used
INIT_B	in	L2	PS_1V8	FPGA Init
JTAGEN	-	E5	3V_D	JTAG Enable
LED_FP_4	out	M4	3.3V	Front panel LED
LP_GOOD	in	H13	3V_D	LP Power Good
M10_RST	-	A7	3V_D	/ currently_not_used
M10_RX	-	C2	3V_D	/ currently_not_used
M10_TX	-	B1	3V_D	/ currently_not_used
MAX_IO1 / IO1	in	N8	3.3V	I²C SCL in, ZynqMP Pin G18
MAX_IO10	-	M10	3.3V	/ currently_not_used
MAX_IO2 / IO2	out	N7	3.3V	I²C SCL out, ZynqMP Pin G19
MAX_IO3 / IO3	in	M9	3.3V	I²C SDA in, ZynqMP Pin K18
MAX_IO4 / IO4	out	M8	3.3V	I²C SDA out, ZynqMP Pin H19
MAX_IO5 / IO5	in	M12	3.3V	User LED in, ZynqMP Pin J17
MAX_IO6	-	M13	3.3V	/ currently_not_used
MAX_IO7	-	N9	3.3V	/ currently_not_used
MAX_IO8	-	N10	3.3V	/ currently_not_used
MAX_IO9	-	M11	3.3V	/ currently_not_used
MIO22	out	M3	PS_1V8	UART out
MIO23	in	M2	PS_1V8	UART in
MIO24	-	L3	PS_1V8	/ currently_not_used
MIO25	-	H5	PS_1V8	/ currently_not_used
MR	out	K10	3V_D	Supervisor Reset out
N.C.	-	J5	3.3V	/ currently_not_used
N.C.	-	J6	3.3V	/ currently_not_used
N.C.	-	J7	3.3V	/ currently_not_used
N.C.	-	J8	3.3V	/ currently_not_used
N.C.	-	K5	3.3V	/ currently_not_used
N.C.	-	K6	3.3V	/ currently_not_used
N.C.	-	K7	3.3V	/ currently_not_used
N.C.	-	K8	3.3V	/ currently_not_used
N.C.	-	L4	3.3V	/ currently_not_used
N.C.	-	L5	3.3V	/ currently_not_used
N.C.	-	M5	3.3V	/ currently_not_used
N.C.	-	M7	3.3V	/ currently_not_used

N.C.	-	N4	3.3V	/ currently_not_used
N.C.	-	N5	3.3V	/ currently_not_used
N.C.	-	N6	3.3V	/ currently_not_used
N.C.	-	L10	3.3V	/ currently_not_used
N.C.	-	L11	3.3V	/ currently_not_used
N.C.	-	N12	3.3V	/ currently_not_used
nCONF	-	E7	3V_D	/ currently_not_used
nSTATUS	-	C4	3V_D	/ currently_not_used
ON_GT_L	out	J12	3V_D	GT_L Power Enable
ON_GT_R	out	K12	3V_D	GT_R Power Enable
PG_DDR	in	H8	3V_D	DDR Power Good
PG_GT_L	in	H9	3V_D	GT_L Power Good
PG_GT_R	in	G12	3V_D	GT_R Power Good
PG_PL	in	L13	3V_D	PL Power Good
PG_PSGT	in	K11	3V_D	PSGT Power Good
PLL_RST	out	K2	PS_1V8	PLL Chip Reset
PROG_B	out	J2	PS_1V8	FPGA PROG_B
PSON	-	D6	3V_D	/ currently_not_used
RP_SCL	-	E1	3V_D	/ currently_not_used
RP_SDI	-	G4	3V_D	/ currently_not_used
RP_SDO	-	F4	3V_D	/ currently_not_used
RP_SL	-	F1	3V_D	/ currently_not_used
RST	-	B5	3V_D	/ currently_not_used
RST_PRST	-	A8	3V_D	/ currently_not_used
RST_PRST_R	-	B10	3V_D	/ currently_not_used
RST_R	-	D8	3V_D	/ currently_not_used
SATA_SCL	-	G2	3V_D	/ currently_not_used
SATA_SDI	-	F6	3V_D	/ currently_not_used
SATA_SDO	-	F5	3V_D	/ currently_not_used
SATA_SL	-	G1	3V_D	/ currently_not_used
SMB_SCL	inout	E3	3V_D	I²C SCL
SMB_SCL_R	out	E4	3V_D	I²C SCL Pullup Enable
SMB_SDA	inout	C1	3V_D	I²C SDA
SMB_SDA_R	out	D1	3V_D	I²C SDA Pullup Enable
SRST_B	out	H4	PS_1V8	FPGA SRST_B
SW4	in	A5	3V_D	Dip Switch
SYSEN	-	D7	3V_D	/ currently_not_used
USR_BTN	in	J10	3V_D	Front panel button
WAKE	-	A9	3V_D	/ currently_not_used
WAKE_R	-	A10	3V_D	/ currently_not_used

Functional Description

Power

System Controller provides control and status information for main power rails. By default all power rails are ON, the user can manipulate power using I²C interface, see Memory map table.

Reset

System controller generates a reset pulse to supervisor chip U69 when front panel button S3 is pressed.

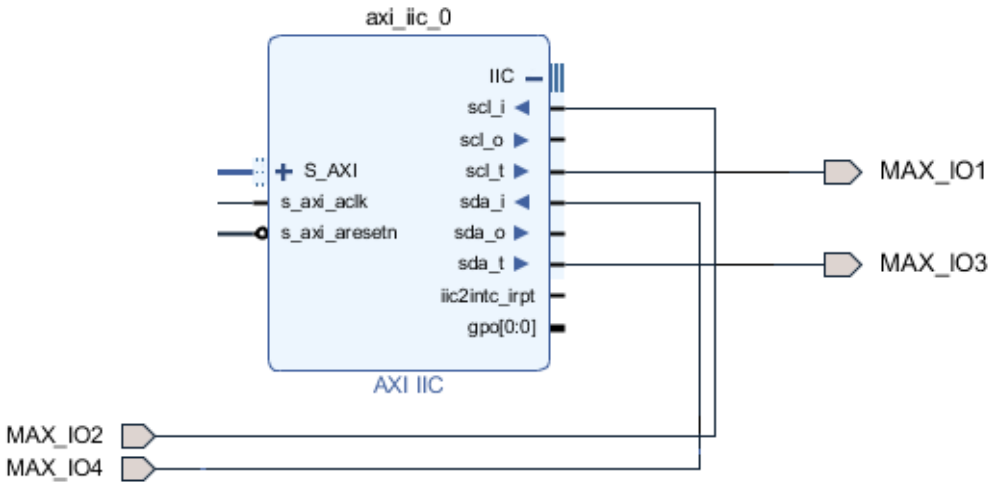
JTAG

JTAG interface from FTDI controller passes through System Controller to FPGA.

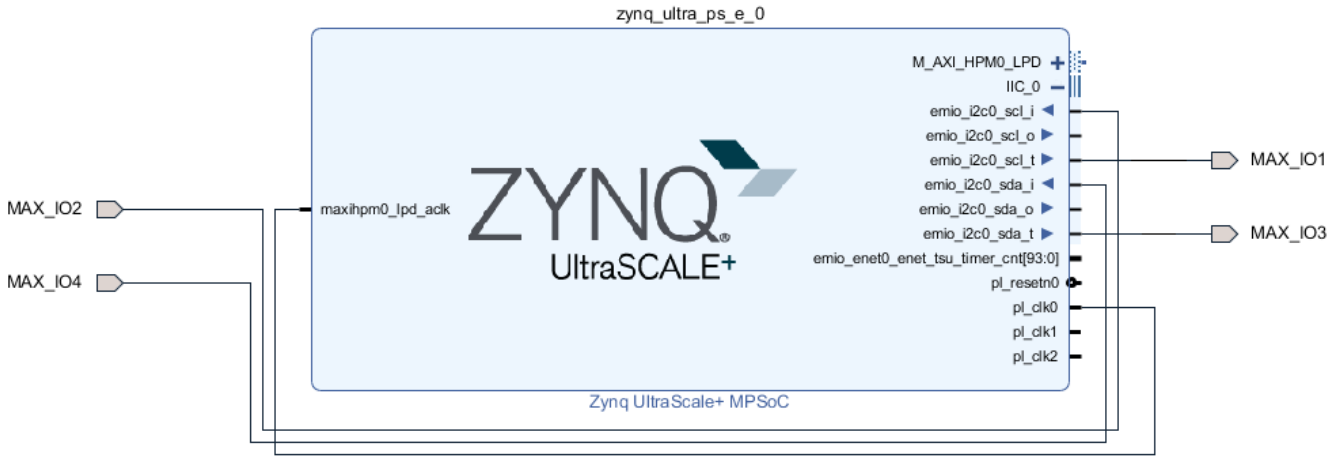
I²C Interface

To use SC I²C interface corresponding connection should be configured in the FPGA project. There are 2 standard I²C interface controllers, which can be used AXI_IIC or Zynq UltraScale+ MPSoC integrated I²C controller.

AXI_IIC



Zynq UltraScale+ MPSoC integrated I²C controller



Project XDC file should contain

```
set_property PACKAGE_PIN G18 [get_ports {MAX_IO1}]
set_property PACKAGE_PIN G19 [get_ports {MAX_IO2}]
set_property PACKAGE_PIN K18 [get_ports {MAX_IO3}]
set_property PACKAGE_PIN H19 [get_ports {MAX_IO4}]
set_property IOSTANDARD LVCMOS33 [get_ports MAX_IO*]
set_property PULLUP true [get_ports {MAX_IO2}]
set_property PULLUP true [get_ports {MAX_IO4}]
```

With this configuration, I²C device with address 0x20 should be visible on I²C bus

```
root@petalinux:~# i2cdetect -r -y 0
     0  1  2  3  4  5  6  7  8  9  a  b  c  d  e  f
00:          -- -- -- -- -- -- -- -- -- -- -- -- --
10: -- -- -- -- -- -- -- -- -- -- -- -- -- -- -- --
20: 20 -- -- -- -- -- -- -- -- -- -- -- -- -- -- --
30: -- -- -- -- -- -- -- -- -- -- -- -- -- -- -- --
40: -- -- -- -- -- -- -- -- -- -- -- -- -- -- -- --
50: -- -- -- -- -- -- -- -- -- -- -- -- -- -- -- --
60: -- -- -- -- -- -- -- -- -- -- -- -- -- -- -- --
70: -- -- -- -- -- -- -- --
root@petalinux:~#
```

This device is an emulation of TCA6416 I²C GPIO Chip. GPIO input and output pins are used to get status and control the system.

Memory map

Address	Register	Description

0	Input Port 0	Power status register: Bit 0 - LP_PGOOD Bit 1 - PG_PL Bit 2 - PG_PSGT Bit 3 - PG_GT_L Bit 4 - PG_GT_R Bit 5 - PG_DDR Bit 6 - AVDD OV/UV Bit 7 - Not Used "0"
1	Input Port 1	FAN Status register Bits 7:0 - FAN RPM/1000 (Nominal Sepa HFB44B-12A speed is 8000 RPM)
2	Output Port 0	Control register 0 Bits 1:0 - LED Control (Default "01") Bit 2 - SMB Strong Pull-Up Enable (Default "1") Bit 3 - Enable DAC1 Power (Default "1") Bit 4 - Enable DAC2 Power (Default "1") Bit 5 - Enable DAC3 Power (Default "1") Bit 6 - Enable DAC4 Power (Default "1") Bit 7 - Enable FPD Power (Default "1")
3	Output Port 1	Control register 1 Bit 0 - Enable LPD Power (Default "1") Bit 1 - Enable DDR Power (Default "1") Bit 2 - Enable PSGT Power (Default "1") Bit 3 - Enable GT_L Power (Default "1") Bit 4 - Enable GT_R Power (Default "1") Bit 5 - Enable FAN Power (Default "1") (Works only if 4-wire FAN is used) Bit 6 - Enable AVDD Power (Default "1") Bit 7 - System reset (Default "0", Reset by rising edge)

LED Control

Bits [1:0]	Mode
"00"	LED4 is OFF
"01"	LED4 is Power indicator
"10"	LED4 is User LED (connected to IO5)

"11"	LED4 is ON

Power Indicator

Behavior	Description
OFF	No power or SC failure
1 Pulse (*ooooooo)	PSGT Power is not OK
2 Pulses (**oooooo)	DDR Power is not OK
3 Pulses (***ooooo)	LP Power is not OK
4 Pulses (****oooo)	GT_L Power is not OK
5 Pulses (*****ooo)	GT_R Power is not OK
6 Pulses (******oo)	PL Power is not OK
ON	No power problems detected

I²C GPIO registers can be operated with directly, using Linux i2cset and i2cget commands

```
root@petalinux:~# # Disable LED4
root@petalinux:~# i2cset -y 0 0x20 2 0xFC
root@petalinux:~# # Get Power status
root@petalinux:~# i2cget -y 0 0x20 0 b
0x3f
root@petalinux:~# # Get FAN RPM/1000
root@petalinux:~# i2cget -y 0 0x20 1 b
0x08
```

or I²C GPIO device driver can be instantiate in Linux device tree (project-spec/meta-user/recipes-bsp/device-tree/files/system-user.dtsi).

```
&i2c0 {
        tca6416: tca6416@21 {
                compatible = "ti,tca6416";
                reg = <0x20>;
                gpio-controller;
                #gpio-cells = <2>;
        };
};
```

LED

The System Controller control D4 LED (front panel green rightmost LED). By default, it act like power status indicator see "Power Indicator" table in "I²C interface" section.

Appx. A: Change History and Legal Notices

Revision Changes

RE02 to REV03

- Add I²C GPIO core
- FAN Control/FAN Status
- Power control

RE03 to REV04

- BUGFIX Reset

Document Change History

To get content of older revision got to "Change History" of this page and select older document revision number.

Date	Document Revision	CPLD Firmware Revision	Supported PCB Revision	Authors	Description
	Error rendering macro 'page-info' Ambiguous method overloading for method jdk.proxy279.$Proxy4022#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] Unknown macro: 'metadata'	REV04	REV02	**Error rendering macro 'page-info'** Ambiguous method overloading for method jdk.proxy279.$Proxy4022#hasContentLevelPermission. Cannot	• REV04 finished • Firmware release on 2018-10-24

Error rendering macro 'page-info'

Ambiguous method overloading for method jdk.proxy279.$Proxy4022#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]

resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.

				lang. String, class com. atlassian. confluence. core. ContentEntityObject] [interface com. atlassian. user. User, class java. lang. String, class com. atlassian. confluence. core. ContentEntityObject]	
2018-10-10	v.20	REV03	REV02	Oleksandr Kiyenko	• REV03 finished • Firmware release on 2018-10-10

2018-08-15	v.3	REV02	REV02	Antti Lukats	• initial release
	All			**Error rendering macro 'page-info'** Ambiguous method overloading for method jdk.proxy279.$Proxy4022#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.	

String, class com. atlassi an. conflue nce. pages. Page] due to overla pping prototy pes betwee n: [interfa ce com. atlassi an. conflue nce. user. Conflu enceU ser, class java. lang. String, class com. atlassi an. conflue nce. core. Conten

				tEntity Object] [interfa ce com. atlassi an. user. User, class java. lang. String, class com. atlassi an. conflue nce. core. Conten tEntity Object]	

Appx. A: Legal Notices