TE0725 HyperRAM

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Error rendering macro 'toc'

[com.ctc.wstx.exc.WstxLazyException] com.ctc.wstx.exc.WstxParsingException: String '--' not allowed in comment (missing '>'?) at [row, col {unknown-source}]: [39,-1115]

Overview

MicroBlaze Design with HyperRAM memory test example.

This reference designs is bundled with a FREE evaluation edition of the commercially proven, low-cost, low-circuit area, high performance, HyperBus Memory Controller (HBMC) IP supplied by Synaptic Laboratories Ltd. Synaptic Labs HBMC IP is commercially proven in both Intel and Xilinx projects, and was selected by Intel. This FREE HBMC IP evaluation license never expires, and no customer registration or NIC ID is required.

You can check for and obtain the latest version of the FREE evaluation HBMC IP from S/Labs website for Xilinx on S/Labs HBMC IP (Free Trail IP) . Please send your HBMC IP support questions to info@synaptic-labs.com

Key Features

- MicroBlaze
- QSPI
- I2C
- UART
- HyperRAM
- S/Labs HBMC IP (Free Trail IP)

Revision History

Date	Vivado	Project Built	Authors	Description
2018-08-09	2018.2	TE0725-HyperRAM_noprebuilt-vivado_2018.2-build_02_20180809122634.zip TE0725-HyperRAM-vivado_2018.2-build_02_20180809122623.zip	John Hartfiel	• 2018.2 update • new HBMC IP version (v1_3_57)
2018-06-05	2017.4	TE0725-HyperRAM_noprebuilt-vivado_2017.4-build_10_20180605162539.zip TE0725-HyperRAM-vivado_2017.4-build_10_20180605162425.zip	John Hartfiel	• initial release

Release Notes and Know Issues

Issues	Description	Workaround	To be fixed version
No known issues	---	---	---

Requirements

Software

Software	Version	Note
Vivado	2018.2	needed
SDK	2018.2	needed

Hardware

Basic description of TE Board Part Files is available on TE Board Part Files.

Complete List is available on <design name>/board_files/*_board_files.csv

Design supports following modules:

Module Model	Board Part Short Name	PCB Revision Support	DDR	QSPI Flash	Others	Notes
TE0725-03-15-1C	15_1c	REV01, REV02, REV03	---	32	8MB HypeRAM	
TE0725-03-35-2C	35_2c	REV01, REV02, REV03	---	32	8MB HypeRAM	
TE0725-03-100-2C	100_2c	REV01, REV02, REV03	---	32	8MB HypeRAM	
TE0725-03-100-2CF	100_2c	REV01, REV02, REV03	---	32	8MB HypeRAM	POF assembled
TE0725-03-100-2I9	100_2i	REV01, REV02, REV03	---	32	8MB HypeRAM	

Design supports following carriers:

Carrier Model	Notes

Additional HW Requirements:

Additional Hardware	Notes
TE0790 JTAG Programmer	It's not recommended to use TE0790 for power supply(TE0790 TRM#PowerandPower-OnSequence)
External power supply	

Content

For general structure and of the reference design, see Project Delivery

Design Sources

Type	Location	Notes
Vivado	<design name>/block_design <design name>/constraints <design name>/ip_lib	Vivado Project will be generated by TE Scripts
SDK/HSI	<design name>/sw_lib	Additional Software Template for SDK/HSI and apps_list.csv with settings for HSI

Additional Sources

Type	Location	Notes

Prebuilt

File	File-Extension	Description
BIT-File	*.bit	FPGA (PL Part) Configuration File
Diverse Reports	---	Report files in different formats
Hardware-Platform-Specification-Files	*.hdf	Exported Vivado Hardware Specification for SDK/HSI and PetaLinux
LabTools Project-File	*.lpr	Vivado Labtools Project File
MCS-File	*.mcs	Flash Configuration File with Boot-Image (MicroBlaze or FPGA part only)
MMI-File	*.mmi	File with BRAM-Location to generate MCS or BIT-File with *.elf content (MicroBlaze only)
Software-Application-File	*.elf	Software Application for Zynq or MicroBlaze Processor Systems

Download

Reference Design is only usable with the specified Vivado/SDK/PetaLinux/SDx version. Do never use different Versions of Xilinx Software for the same Project.

Reference Design is available on:

- TE0725 "HyperRAM" Reference Design

Design Flow

Reference Design is available with and without prebuilt files. It's recommended to use TE prebuilt files for first lunch.

Trenz Electronic provides a tcl based built environment based on Xilinx Design Flow.

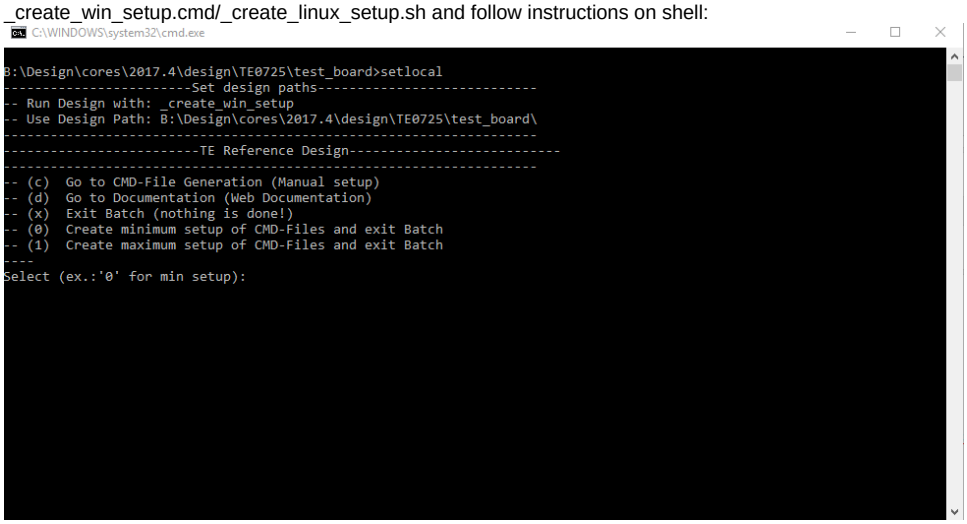
See also:

- Vivado/SDK/SDSoC#XilinxSoftware-BasicUserGuides
- Vivado Projects
- Project Delivery.

The Trenz Electronic FPGA Reference Designs are TCL-script based project. Command files for execution will be generated with "_create_win_setup.cmd" on Windows OS and "_create_linux_setup.sh" on Linux OS.

TE Scripts are only needed to generate the vivado project, all other additional steps are optional and can also executed by Xilinx Vivado/SDK GUI. For currently Scripts limitations on Win and Linux OS see: Project Delivery Currently limitations of functionality

1. _create_win_setup.cmd/_create_linux_setup.sh and follow instructions on shell:



2. Press 0 and enter for minimum setup
3. (optional Win OS) Generate Virtual Drive or use short directory for the reference design (for example x:\<design name>)
4. Create Project
    a. Select correct device and Xilinx install path on "design_basic_settings.cmd" and create Vivado project with "vivado_create_project_guimode.cmd"
    Note: Select correct one, see TE Board Part Files
5. Create HDF and export to prebuilt folder
    a. Run on Vivado TCL: TE::hw_build_design -export_prebuilt
    Note: Script generate design and export files into \prebuilt\hardware\<short dir>. Use GUI is the same, except file export to prebuilt folder
6. Generate Programming Files with HSI/SDK
    a. Run on Vivado TCL: TE::sw_run_hsi
    Note: Scripts generate applications and bootable files, which are defined in "sw_lib\apps_list.csv"
    b. (alternative) Start SDK with Vivado GUI or start with TE Scripts on Vivado TCL: TE::sw_run_sdk
    Note: See SDK Projects
7. Copy Application (memory_tests.elf) into \firmware\microblaze_0\
8. Regenerate Design:
    a. Run on Vivado TCL: TE::hw_build_design -export_prebuilt
    Note: App from Firmware folder will be add into BlockRAM. If you add other app, you must select *.elf manually on Vivado
    b. (alternative) Use SDK or Vivado to update generate Bitfile with new Application and regenerate mcs manually.

Launch

Programming

⚠ Check Module and Carrier TRMs for proper HW configuration before you try any design.

Xilinx documentation for programming and debugging: Vivado/SDK/SDSoC-Xilinx Software Programming and Debugging

QSPI

1. Connect JTAG and power on PCB
2. (if not done) Select correct device and Xilinx install path on "design_basic_settings.cmd" and create Vivado project with "vivado_create_project_guimode.cmd" or open with "vivado_open_project_guimode.cmd", if generated.
3. Type on Vivado Console: TE::pr_program_flash_mcsfile
   Note: Alternative use SDK or setup Flash on Vivado manually
4. Reboot (if not done automatically)

SD

Not used on this Example.

JTAG

1. Connect JTAG and power on PCB
2. (if not done) Select correct device and Xilinx install path on "design_basic_settings.cmd" and create Vivado project with "vivado_create_project_guimode.cmd" or open with "vivado_open_project_guimode.cmd", if generated.
3. Open Vivado HW Manager
4. Program Bitfile

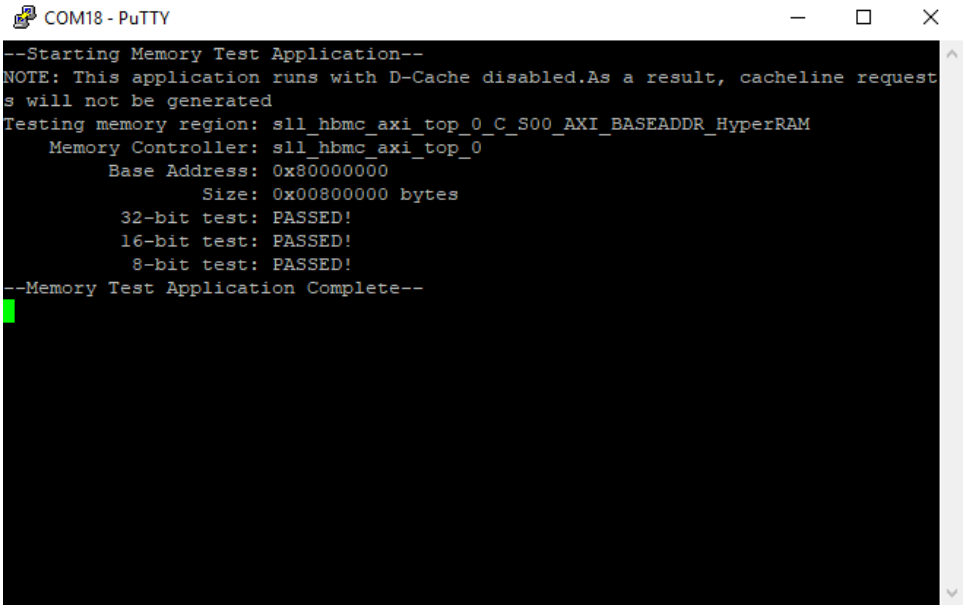
Usage

> HBMC IP is a 10 minute run-time limited evaluation version of the full-edition

1. Prepare HW like described on section Programming
2. Connect UART USB (most cases same as JTAG)
3. Power On PCB (Do not restart, if you use Bitfile programming)
   Note: FPGA Loads Bitfile from Flash

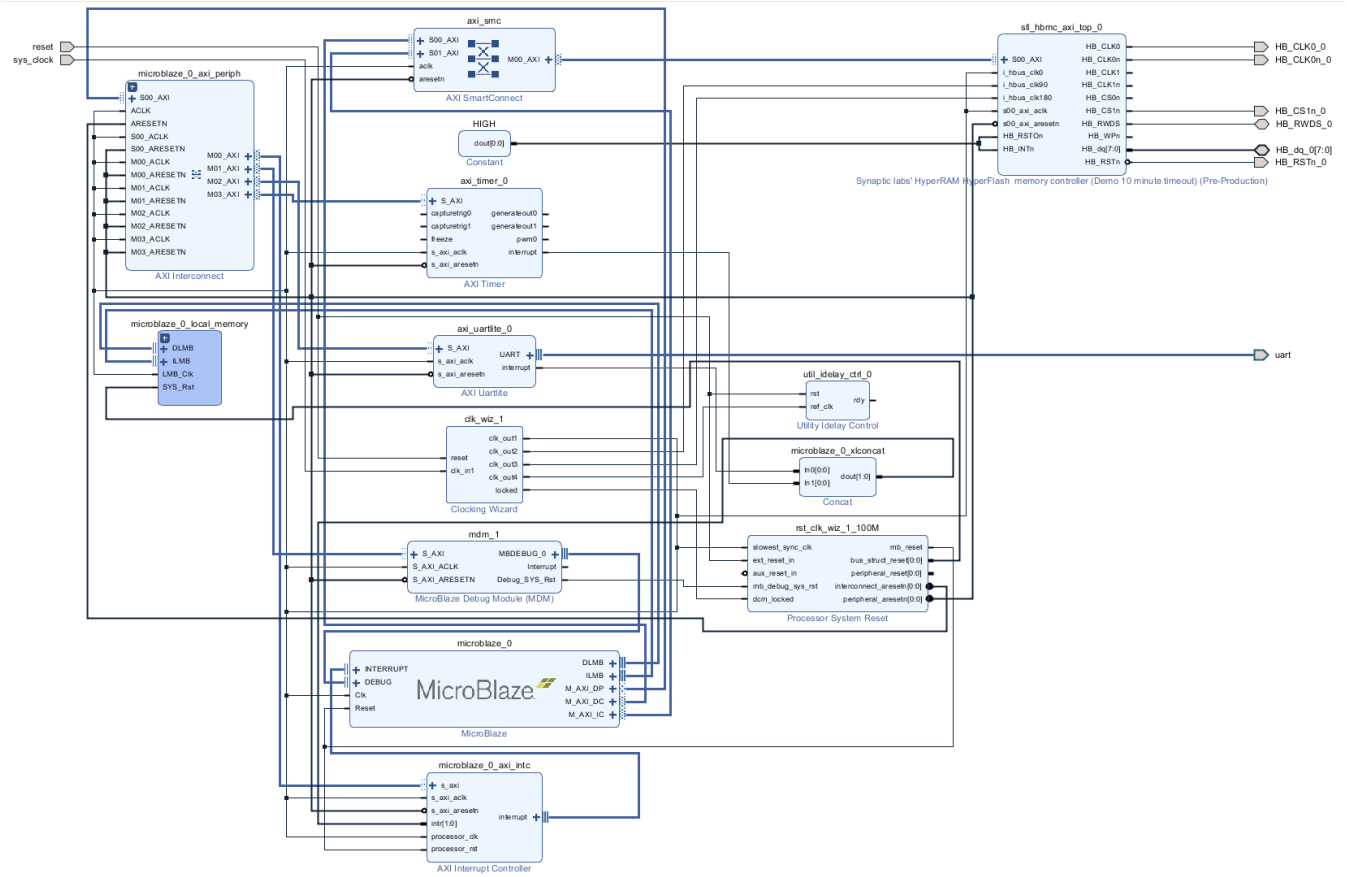
UART

1. Open Serial Console (e.g. putty)
   a. Speed: 9600
   b. COM Port: Win OS, see device manager, Linux OS see dmesg |grep tty (UART is *USB1)
2. Uart Console:
   Xilinx Memory test on HyperRAM



System Design - Vivado

Block Design



Constrains

Basic module constrains

_i_bitgen_common.xdc

```
set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design]
set_property BITSTREAM.CONFIG.CONFIGRATE 50 [current_design]
set_property CONFIG_VOLTAGE 3.3 [current_design]
set_property CFGBVS VCCO [current_design]
set_property BITSTREAM.CONFIG.SPI_32BIT_ADDR YES [current_design]
set_property BITSTREAM.CONFIG.SPI_BUSWIDTH 4 [current_design]
set_property BITSTREAM.CONFIG.M1PIN PULLNONE [current_design]
set_property BITSTREAM.CONFIG.M2PIN PULLNONE [current_design]
set_property BITSTREAM.CONFIG.M0PIN PULLNONE [current_design]

set_property BITSTREAM.CONFIG.USR_ACCESS TIMESTAMP [current_design]
```

Design specific constrain

_i_hyperram.xdc

```
set_property PACKAGE_PIN A13 [get_ports HB_CLK0_0]
set_property PACKAGE_PIN A14 [get_ports HB_CLK0n_0]

set_property PACKAGE_PIN E17 [get_ports {HB_dq_0[0]}]
set_property PACKAGE_PIN B17 [get_ports {HB_dq_0[1]}]
set_property PACKAGE_PIN F18 [get_ports {HB_dq_0[2]}]
set_property PACKAGE_PIN F16 [get_ports {HB_dq_0[3]}]
set_property PACKAGE_PIN G17 [get_ports {HB_dq_0[4]}]
set_property PACKAGE_PIN D18 [get_ports {HB_dq_0[5]}]
set_property PACKAGE_PIN B18 [get_ports {HB_dq_0[6]}]
set_property PACKAGE_PIN A16 [get_ports {HB_dq_0[7]}]


set_property PACKAGE_PIN E18 [get_ports HB_RWDS_0]

set_property PACKAGE_PIN D17 [get_ports HB_CS1n_0]
set_property PACKAGE_PIN J17 [get_ports HB_RSTn_0]

#set_property PACKAGE_PIN A18 [get_ports HB_CS0n_0 ]
#set_property PACKAGE_PIN J18 [get_ports HB_INTn_0 ]
#set_property PACKAGE_PIN C17 [get_ports HB_RSTOn_0]


#
# FPGA Pin Voltage assignment
#
set_property IOSTANDARD LVCMOS18 [get_ports HB_CLK0_0]
set_property IOSTANDARD LVCMOS18 [get_ports HB_CLK0n_0]
set_property IOSTANDARD LVCMOS18 [get_ports {HB_dq_0[*]}]
set_property IOSTANDARD LVCMOS18 [get_ports HB_CS1n_0]
set_property IOSTANDARD LVCMOS18 [get_ports HB_RSTn_0]
set_property IOSTANDARD LVCMOS18 [get_ports HB_RWDS_0]

#set_property IOSTANDARD LVCMOS18 [get_ports HB_CS0n_0]
#set_property IOSTANDARD LVCMOS18 [get_ports HB_INTn_0]
#set_property IOSTANDARD LVCMOS18 [get_ports HB_RSTOn_0]

#set_property PULLUP true [get_ports HB_RSTOn_0]
#set_property PULLUP true [get_ports HB_INTn_0]

#
#Hyperbus Clock - change according to clk pin on PLL
#
create_generated_clock -name clk_0   -source [get_pins msys_i/clk_wiz_0/inst/mmcm_adv_inst/CLKIN1] -
master_clock sys_clock [get_pins msys_i/clk_wiz_0/inst/mmcm_adv_inst/CLKOUT0]
create_generated_clock -name clk_90  -source [get_pins msys_i/clk_wiz_0/inst/mmcm_adv_inst/CLKIN1] -
master_clock sys_clock [get_pins msys_i/clk_wiz_0/inst/mmcm_adv_inst/CLKOUT1]
create_generated_clock -name clk_180 -source [get_pins msys_i/clk_wiz_0/inst/mmcm_adv_inst/CLKIN1] -
master_clock sys_clock [get_pins msys_i/clk_wiz_0/inst/mmcm_adv_inst/CLKOUT2]

#
#100Mhz clock freqeuncy - change accordingly
#
```

```
set hbus_freq_ns   10

set dqs_in_min_dly -0.5
set dqs_in_max_dly  0.5

set HB_dq_ports    [get_ports HB_dq_0[*]]

#
#Create RDS clock and RDS virtual clock
#
create_clock -period $hbus_freq_ns -name rwds_clk      [get_ports HB_RWDS_0]
create_clock -period $hbus_freq_ns -name virt_rwds_clk

#
#Input Delay Constraint -  HB_RWDS-HB_DQ
#
set_input_delay -clock [get_clocks virt_rwds_clk]             -max ${dqs_in_max_dly} ${HB_dq_ports}
set_input_delay -clock [get_clocks virt_rwds_clk] -clock_fall -max ${dqs_in_max_dly} ${HB_dq_ports} -add_delay

set_input_delay -clock [get_clocks virt_rwds_clk]             -min ${dqs_in_min_dly} ${HB_dq_ports} -add_delay
set_input_delay -clock [get_clocks virt_rwds_clk] -clock_fall -min ${dqs_in_min_dly} ${HB_dq_ports} -add_delay

set_multicycle_path -setup -end -rise_from [get_clocks virt_rwds_clk] -rise_to [get_clocks rwds_clk] 0
set_multicycle_path -setup -end -fall_from [get_clocks virt_rwds_clk] -fall_to [get_clocks rwds_clk] 0

set_false_path  -fall_from [get_clocks virt_rwds_clk] -rise_to [get_clocks rwds_clk] -setup
set_false_path  -rise_from [get_clocks virt_rwds_clk] -fall_to [get_clocks rwds_clk] -setup
set_false_path  -fall_from [get_clocks virt_rwds_clk] -fall_to [get_clocks rwds_clk] -hold
set_false_path  -rise_from [get_clocks virt_rwds_clk] -rise_to [get_clocks rwds_clk] -hold

set_false_path -from [get_clocks clk_0] -to [get_clocks rwds_clk]
set_false_path -from [get_clocks rwds_clk] -to [get_clocks clk_0]

#
#Output Delay Constraint -  HB_CLK0-HB_DQ
#

create_generated_clock -name HB_CLK0_0 -source [get_pins */*/*/U_IO/U_CLK0/dq_idx_[0].ODDR_inst/C] -multiply_by
1 -invert [get_ports HB_CLK0_0]

set_output_delay -clock [get_clocks HB_CLK0_0] -min -1.000 ${HB_dq_ports}
set_output_delay -clock [get_clocks HB_CLK0_0] -max  1.000 ${HB_dq_ports}
set_output_delay -clock [get_clocks HB_CLK0_0] -min -1.000 ${HB_dq_ports} -clock_fall -add_delay
set_output_delay -clock [get_clocks HB_CLK0_0] -max  1.000 ${HB_dq_ports} -clock_fall -add_delay


set_false_path -from [get_pins */*/*/U_HBC/*/dq_io_tri_reg/C] -to ${HB_dq_ports}

set_false_path -from * -to [get_pins */*/inst/*/i_iavs0_270_rstn_1_reg/CLR]
set_false_path -from * -to [get_pins */*/inst/*/i_iavs0_270_rstn_2_reg/CLR]
set_false_path -from * -to [get_pins */*/inst/*/i_iavs0_270_rstn_3_reg/CLR]
```

Software Design - SDK/HSI

For SDK project creation, follow instructions from:

SDK Projects

Application

memory_tests

Xilinx default memory test.

Additional Software

No additional software is needed.

Appx. A: Change History and Legal Notices

Document Change History

To get content of older revision got to "Change History" of this page and select older document revision number.

Date	Document Revision	Authors	Description
2018-08-09	v.4 Unknown macro: 'metadata'	John Hartfiel	• 2018.2 release
06 Jun 2018	v.3	John Hartfiel	• Documentation update
05 Jun 2018	v.2	John Hartfiel	• 2017.4 release
2018-05-06	v.1	John Hartfiel	• Initial release
	All	John Hartfiel	

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2019-06-07