

TE Board Part Files

Most of the TE modules are available in different assembly options. Assembly option with different FPGA/SOC devices or other DDR sizes need an own board part file. In some cases also a PCB revision changes or a special carrier module combination needs a separate board part.

It's recommended to use the board part files only for this Vivado Version, for which it has been provided. Depending on the Schema Version of the XML-Files and Xilinx IP definitions, it is possible to use them with other Vivado versions, see Xilinx ug895.

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Naming Conventions and Version

This Naming Convention will be used for the most Vivado 2016.2 Board Part Files and newer one.

Board Part Files consists on a base folder, a version sub folder with three xml files and one picture:

- Every assembly option of a module/carrier series where FPGA-Typ (Size, Speed/Temperature Grade) is changed, gets a new base folder.
- Every other assembly option or PCB-revision change, which has affects on the reference design settings, gets a new version sub folder.

Board Part Base Folder

Board Part Names of the base folder consists of max. three parts separated by underline character.

| | Usage of the part of name | Example 1 | Example 2 | Example 3 | Example 4 |
|-------------------------------------|---------------------------|-----------|-----------|-----------|-----------|
| Name of the PCB Series | Always | TE0726 | TE0745 | TE0720 | TE0711 |
| FPGA Size | Optional | | 30 | | 35 |
| FPGA Speed/Temperature Grade | Optional | | | 1C | 2C |

Board Part Version Folder

Version folder Name consists on a major and minor number separated by a dot (<major>.<minor>, example 1.0) Different Version folder means:

| | |
|--------------|---|
| Major | <ul style="list-style-type: none">• Changes on assembly option, which has effects on the reference design, for example DDR Size• Board Part for special Carrier/Module combination |
| Minor | <ul style="list-style-type: none">• Changes on PCB-Revision, which has effects on the reference design |

Attention: Changes on the settings of the TE Board Part Files by itself are not under version control at the moment, like described in Xilinx ug895. XML file includes a comment header with the date of the last change of the selected file.

Location

Board Part Files will be delivered with our Reference Designs on our https://shop.trenz-electronic.de/Download/?path=Trenz_Electronic/<group>/<form factor>/<module_name>/Reference_Design/<vivado_version>/<design_name>.

Board Part Files are locate in the sub folder <design_name>/board_files/ of the downloadable Reference Design. For detailed information of the zip-file folder structure see: [Project Delivery - Directory Structure](#).

This folder includes also a *_board_files.csv file with a list of all available board parts. This list is only used by TE-Scripts.

Select Correct Board Part Files

- Check <design_name>/board_files/<board_series>_board_files.csv for available board part of the reference design:
 - The table shows all available board parts, which are delivered with the reference design
 - "Product ID" is only the newest one and in the most cases the same as the model number on your order or shop page.
 - Revision number of the PRODDID (-03- in this example) is the last one, which was available on last board part update. If there is no special board part for older revisions, this will be backward compatible. Please verify this on Vivado, see 4.
 - "Part Name" is the FPGA device setting of Vivado for the assembly variant
 - "Board Name" is the hole board part name
 - "Short Name" is the name for the board part specific sub folders in the reference design
 - "Zynq Flash Typ" is the setting to configure the Flash via SDK
 - "FPGA Flash Typ" is the setting to configure the Flash via Vivado (first part only), the second and third part are QSPI mode and memory size in MB
 - "Note" is for additional information
 - "PCB": supported PCB Revisions(dot is separator)
 - "B,I,P": differences between board part files (excepted FPGA device)
 - "R": Memory option and size

```

TE0720xxw1_Board.csv
CSV_VERSION=1.3
#Comment: do not change matrix position or remove CSV_VERSION:
# ID , PRODDID , PARTNAME , BOARDNAME , SHORTNAME , ZYNQFLASH_TYP , FPGAFLASH_TYP , Note
4 1 , tw0720-03-2if , xc7z020clg484-2 , xc7z020_2ipart0:1.0 , tw0720_2if , qspi_single , #25f1256xxxxxxxxx0-mp1-x1_x2_x4f18P1x4f132 , PCB:2.3|B:1|I:1|P:1|R:1|S:0MB
5 2 , tw0720-03-1cr , xc7z020clg484-1 , xc7z020_1ipart0:2.0 , tw0720_1cr , qspi_single , #25f1256xxxxxxxxx0-mp1-x1_x2_x4f18P1x4f132 , PCB:2.3|B:1|I:1|P:2|R:1|S:0MB
6 3 , tw0720-03-1qf , xc7z020clg484-1q , xc7z020_1qpart0:1.0 , tw0720_1qf , qspi_single , #25f1256xxxxxxxxx0-mp1-x1_x2_x4f18P1x4f132 , PCB:2.3|B:1|I:1|P:1|R:1|S:0MB
7 4 , tw0720-03-1lif , xc7z020clg484-1 , xc7z020_1lipart0:1.0 , tw0720_1lif , qspi_single , #25f1256xxxxxxxxx0-mp1-x1_x2_x4f18P1x4f132 , PCB:2.3|B:1|I:1|P:3|R:1|S:2MB
8 5 , tw0720-03-1cf , xc7z020clg484-1 , xc7z020_1cfpart0:1.0 , tw0720_1cf , qspi_single , #25f1256xxxxxxxxx0-mp1-x1_x2_x4f18P1x4f132 , PCB:2.3|B:1|I:1|P:1|R:1|S:0MB
9 6 , tw0720-03-2ef , xc7z020clg484-2 , xc7z020_2efpart0:1.0 , tw0720_2ef , qspi_single , #25f1256xxxxxxxxx0-mp1-x1_x2_x4f18P1x4f132 , PCB:2.3|B:1|I:1|P:1|R:1|S:0MB
10 7 , tw0720-03-07a , xc7z014clg484-1 , xc7z014_7apart0:1.0 , tw0720_7a , qspi_single , #25f1256xxxxxxxxx0-mp1-x1_x2_x4f18P1x4f132 , PCB:2.3|B:1|I:1|P:4|R:1|S:0MB
    
```

- Check your order number and/or TE shop page to get module information of your PCB:
 - <https://shop.trenz-electronic.de/en/Products/Trenz-Electronic/<device familie>/<TE module serie>>
 - "Model Overview" shows the basic difference between the assembly options, in the most cases different footprint compatible FPGAs or RAM size. Assembly options (like different connector) which has no affect on board parts settings, has no separate board part files.

Neue Produkte

% SALE %

Trenz Electronic

- Trägerboards
- 4x5 SoMs
- Starter Kits
- Pmod-kompatibel
- Open Hardware
- TE08XX - Zynq UltraScale+
- TE084X - Kintex UltraScale
- TE07XX - Zynq SoC
- TE0715 - Zynq SoC
- TE0720 - Zynq SoC
- TE0722 - Zynq SoC
- TE0723 - Zynq SoC

Modellübersicht

| Modell | Formfaktor | FPGA | RAM | Ethernet | Temperaturbereich |
|---------------------|------------|-------------------|-----------------|----------|-------------------|
| TE0720-03-2IF | 4 x 5 cm | XC7Z020-2CLG484I | 1 GByte DDR | 1 GBit | industrial |
| TE0720-03-2IFC3 *1) | 4 x 5 cm | XC7Z020-2CLG484I | 1 GByte DDR | 1 GBit | industrial |
| TE0720-03-1L1F *2) | 4 x 5 cm | XC7Z020-L1CLG484I | 512 MByte DDR3L | 1 GBit | industrial |
| TE0720-03-1CF | 4 x 5 cm | XC7Z020-1CLG484C | 1 GByte DDR | 1 GBit | commercial |
| TE0720-03-1CR | 4 x 5 cm | XC7Z020-1CLG484C | 256 MByte DDR | 1 GBit | commercial |
| TE0720-03-1QF | 4 x 5 cm | XA7Z020-1CLG484Q | 1 GByte DDR | 1 GBit | automotive |

*1) Dieses Modul ist baugleich mit dem TE0720-xx-2IF, allerdings sind hier anstatt 4mm lediglich 2.5mm Samtec-Stecker verbaut.

*2) Produktion nach Bestellung. Dieses Modell ist bis auf den Speicher (512 DDR3L MByte anstatt 1 GByte DDR SDRAM) baugleich zum TE0720-xx-xIF, ausser dass hier ist ein Xilinx Zynq-7020 SoC XC7Z020-L1CLG484I verbaut ist, der weniger Strom verbraucht.

- Select your board part file on design_basic_settings.cmd/sh:
 - Use unique name from CSV list (see 1.)
 - Unique names are ID or PRODDID (in the most cases) or BOARDNAME or SHORTNAME
 - Revision number of the PRODDID is the last one, which was available on last board part update. If there is no special board part for older revisions, this will be backward compatible. Please verify this on Vivado, see 4.

```

29 #RDN -----
30 #RDN Set Board part number of the project which should be created
31 #RDN "Available Numbers: you can use ID, PRODDID, BOARDNAME or SHORTNAME from 'board_files\TExxx_board_files.csv |ls|' or special name "LAST_ID" to get the board with the highest ID in the *_csv list
32 #RDN --variable is used for project creation and programming
33 #RDN --Example TE0726 Module
34 #RDN --USE ID --USE PRODDID --USE BOARDNAME --USE SHORTNAME
35 #RDN --Set PARTNUMBER=18set PARTNUMBER=tw0726-3m --Set PARTNUMBER=xc7z020_1ipart0:3.1 --Set PARTNUMBER=te0726_m
36 #set PARTNUMBER=LAST_ID ← Select your board part here
    
```

See Reference Design: [Getting Started](#) for more details.

- Create Vivado Project with vivado_create_project_gui mode.cmd/sh

5. Verify your board part selection on Vivado "Project Summary" tap:

The screenshot shows the Vivado Project Summary window with the following sections and annotations:

- Project Settings:**
 - Project name: test_board
 - Project location: B:\SIV\cores\2016_4\design\TE0720\test_board\vivado
 - Product family: Zynq-7000
 - Project part: [ZYNQ-7 TE0720_1 IIF_SVRT PCB: REV02_REV03 \(xc7z020dpg484-1\)](#)
 - Top module name: [mys_xrtapplet](#)
 - Target language: [VHDL](#)
 - Simulator language: [Modelsim](#)
- Board Part:**
 - Display name: ZYNQ-7 TE0720_1 IIF_SVRT PCB: REV02_REV03 (Annotation: Name and supported PCB revisions)
 - Board part name: [trenz.biz:te0720_1:part0:1.0](#) (Annotation: Board name: <base folder>:<part0>:<version folder>)
 - Repository path: B:\SIV\cores\2016_4\design\TE0720\test_board\board_files (Annotation: Repository path of the used board part file)
 - URL: <https://wiki.trenz-electronic.de/display/PD/TE0720+-+GigaZee> (Annotation: Trenz Electronic Wiki URL with detailed PCB description)
 - Board overview: ZYNQ-7 TE0720_1 IIF Board (form factor 4x5 cm) with 512MB DDR3L, 1GB Ethernet, Speed Grade -1 and industrial temperature grade. Supported PCB Revisions: REV02, REV03. (Annotation: Short PCB description and supported PCB revisions)
- Vivado FPGA part:** <family> <size> <package> <speed grade>
- Synthesis:**
 - Status: Not started
 - Messages: No errors or warnings
 - Part: xc7z020dpg484-1 (Annotation: Points to the part name in the implementation section)
 - Strategy: [Vivado Synthesis Defaults](#)
- Implementation:**
 - Status: Not started
 - Messages: No errors or warnings
 - Part: xc7z020dpg484-1
 - Strategy: [Vivado Implementation Defaults](#)
 - Incremental complex: None

Installation

See [Vivado Board Part Installation](#) and [Project Delivery - QuickStart](#)