FAQ

Categories

Trenz Products

EOL of our module series is normally as long as Xilinx and Intel will offer the FPGA/SoC:

- https://shop.trenz-electronic.de/en/Products/Trenz-Electronic/

Passive components (resistors, capacitors) can be changed on the modules without notification. We use different manufacturer and best prices, but in any case the characteristics which are specified in the schematics are the same.

In case other active components will be not longer available, we will replace with footprint compatible equivalent alternatives or we update the PCB to support a equivalent alternatives variant. In case we change such a component, we will create also a new article number, so that you can directly see that something was be updated and we write a PCN

Trenz Electronic provides Module series with different assembly options (FPGA size, speed grade, temperature range, DDR size, QSPI size, eMMC size, less components, different stacking height...)
Identification can be done with the Article number and the corresponding Schematics in the download area of the modules. Module series name and PCB revision is directly printed on the module. Every module has also an unique serial (number on white sticker with QR code on the module), which can be used to identify the whole article number (and thus the assembly options).
Article number style has changed since 2019, so that you can identify main parts also with the article number encoding table:

Article Number Information

Xilinx device information can be requested with the 2D Bare code or Lot code on the device package.

This can be done via Xilinx App:

- https://www.xilinx.com/about/xilinxgo-app-support.html
- https://www.xilinx.com/video/corporate/introduction-2d-barcode-markings.html

Or over web page:

- https://www.xilinx.com/member/2dbarcode.html

In both cases a Xilinx login is needed.

Downloads / Documents

You can lookup for file abbreviations on Documents Naming Conventions.

PCB document is available on our wiki pages and download area.

PCB Design

The maximum power consumption of a module manly depends on the design which is running on the FPGA.

Xilinx provide a power estimator excel sheets to calculate power consumption. It's also possible to generate power consumption of the developed design with Vivado.

Please also observe the TRM of the Trenz Electronic module and the power management of our corresponding carrier boards.

Module pinout files can be generated with our Master Excel Pinout Sheet. You can also use the schematic on our download area.

Trenz Electronic Modules which are offered in the shop are listed on our shop page grouped by FPGA-Family. Wiki overview of the different series is available on Products

See Xilinx Answer Record: AR# 43989

Power sequencing of the FPGA/SoC banks and IOs must be still fulfil restrictions from manufacturer data sheet.

In most case IOs should be enabled after core voltages are powered on. Some module output voltage can be used to enable carrier power regulator for variable bank powers and connected periphery.

See also datasheet power sequencing of the section of the give device:

7 Series:

- https://www.xilinx.com/support/documentation/data_sheets/ds181_Artix_7_Data_Sheet.pdf
- https://www.xilinx.com/support/documentation/data_sheets/ds182_Kintex_7_Data_Sheet.pdf
- https://www.xilinx.com/support/documentation/data_sheets/ds183_Virtex_7_Data_Sheet.pdf
- https://www.xilinx.com/support/documentation/data_sheets/ds187-XC7Z010-XC7Z020-Data-Sheet.pdf
- https://www.xilinx.com/support/documentation/data_sheets/ds191-XC7Z030-XC7Z045-data-sheet.pdf

U/U+ Series:

- https://www.xilinx.com/support/documentation/data_sheets/ds892-kintex-ultrascale-data-sheet.pdf
- https://www.xilinx.com/support/documentation/data_sheets/ds893-virtex-ultrascale-data-sheet.pdf
- https://www.xilinx.com/support/documentation/data_sheets/ds925-zynq-ultrascale-plus.pdf

Xilinx AR#

- https://www.xilinx.com/support/answers/37347.html
- https://www.xilinx.com/support/answers/44225.html

Vivado/SDK/SDSoC/PetaLinux

Links to Xilinx Release Notes are available on Vivado/SDK/SDSoC: Xilinx Software-Product Update Release Notes and Known Issues

Reference Designs will be delivered as scripted project file. Vivado Project files will be generated with these scripts.

Windows and Linux (since Vivado 2016.4) start up command files are available to generate the project: Project Delivery QuickStart

All other options are described on: Vivado Projects - TE Reference Design

Trenz Electronic Board Part Files will be delivered with the reference designs on our download area.They ca be installed in different ways.

1. Select the correct Board Part File: TE Board Part Files
2. Install Board Part Files: Board Part Installation
3. Use Board Part Files: Vivado Board Part Flow

Xilinx Documentation is available on Xilinx Hompage. Some helpful documents are listed on Vivado/SDK/SDSoC.

We provide PetaLinux template projects instead of BSPs for our modules. This template are included in our reference design in the subfolder (os /petalinux).

They are available on our download area. You can lookup for instructions on: PetaLinux KICKstart

Xilinx provide a list with supported functionality and devices on: https://www.xilinx.com/products/design-tools/vivado/vivado-webpack.html

1. Activate ES License with Xilinx License Manager
2. Enable Beta Devices for Vivado
    a. open existing init.tcl (create new one if not exist) in one of this locations:
        i. C:/Xilinx/Vivado/<version>/scripts/
        or
        ii. C:/Users/<user>/AppData/Roaming/Xilinx/Vivado/
    b. Add line: enable_beta_device *

Now Vivado check all Beta Devices, but only Devices with valid license are visible. With Beta Device enable, Vivado need longer startup. Select special beta device is supported too. See Xilinx Forum: Synthesis Failure for ZCU102

Insufficient external power supply can cause this issue. If power supply is insufficient, module restarts and FPGA content is erased. Vivado did not recognize this.

Please check following:

1. Xilinx Programming Cable drivers are installed correctly
2. "hw_server.exe" is terminated on task manage after all xilinx programs are closed. (if not kill this process or restart PC)
3. Board Power Supply is sufficient and on
4. JTAG USB Cable is connected to module and PC

Check if the Quad Enable (QE) bit in the Configuration Register of the flash is set to 1. If the QE-Bit is set or not depends on the last access to the flash.

- This will be done automatically, when you configure Flash with Vivado or SDK and Flash in the design is specified as X4.
- This will be not always done automatically, when you use other software to get access. For example Xilinx barmetal lib doesn't check if the QE bit is set or not.