

4 x 5 SoM Integration Guide

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Power and Signal Pin Assignment

How to Use This Guide

- This guide is split into two tables:
 - **Module Power Connection Table** section shows the power source of the different FPGA banks and components of the different module boards as well as the power and group location on the B2B connectors of the module site.
 - **Carrier Board Power Connection Table** section shows the power source of the B2B connectors with pins, schematic names and available options of the different carrier boards as well as the power location on the B2B connectors of the carrier site.
 - The PCBs have fixed and variable user supplied I/O voltage pins. Variable power supply pins are colored in four groups (VCCIOA, VCCIOB, VCCIOC and VCCIOD).
1. Find your module model on the **Module Power Connection Table** and check the power supply of the different FPGA banks.
 2. If the power supply is variable(colored), go to the **Carrier Board Power Connection Table** and see how it's connected on your carrier board. Often the power source can be selected by jumper, resistor or variable used from other connector pin of the carrier board. So use the schematic name or the component designator from the table to search for the available options in the PCB schematics or TRM.
 3. Additional Master Pinout Viewer/XDC-Generator is available on [Trenz Electronic Download - Pinout](#)

Module Power Connection Table

Group	1				2				3				4				5				6				7				8	9	special	
Module Model	Bank	IOs	Type	Voltage	Bank	IOs	Type	Voltage	Bank	IOs	Type	Voltage	Bank	IOs	Type	Voltage	Bank	IOs	Type	Voltage	Bank	IOs	Type	Voltage	Bank	IOs	Type	Voltage				
TE0710	B15	48	HR	VC CIOA	-	-	-	-	-	-	-	-	B34	50	HR	VC CIOD	B16	6	HR	3.3 V	B14	8	HR	3.3 V	2x 100Mbit ETH							
TE0711	B15	48	HR	VC CIOA	B34	36	HR	VC CIOB	B14	18	HR	3.3 V	B35	50	HR	VC CIOD	B16	6	HR	1.8 V	B14	8	HR	3.3 V	B34	8	HR	VC CIOB	B34(4)	USB		
TE0712	B16	48	HR	VC CIOA	B13	20	HR	VC CIOB	B14	18	HR	3.3 V	B15	50	HR	VC CIOD	B13	6	HR	VC CIOB	B14	8	HR	3.3 V	1x 100Mbit ETH / B13	4	HR	VC CIOB		B14	4x GTP on G2	
TE0713																															4x GTP on G2	
TE0715 with Z-7015	B13	48	HR	VC CIOA	B34	16	HR	VC CIOC	B34	18	HR	VC CIOC	B35	50	HR	VC CIOD	B5 01	6	MIO	1.8 V	B500	8	MIO	3.3 V	1x Gbit ETH				SGMII	USB	4x GTP on G2	

TE0715 with Z-7030	B13	48	HR	VC CIOA	B34	16	HP	VC CIOB	B34	18	HP	VC CIOB	B35	50	HP	VC CIOD	B5	6	MIO	1.8 V	B500	8	MIO	3.3 V	1x Gbit ETH				SGMII	USB	4x GTP on G2	
TE0720	B35	48	HR	VC CIOA	B34	36	HR	VC CIOB	B33	18	HR	VC CIOB	B13	50	HR	VC CIOD	B5	6	MIO	1.8 V	B500	8	MIO	3.3 V	1x Gbit ETH				SGMII	USB		
TE0820*	B66	48	HP	VC CIOA	B65	16	HP	VC CIOB	B65	18	HP	VC CIOB	B64	50	HP	VC CIOD	B5	6	MIO	3.3 V	B5 01	8	MIO	3.3 V	1x Gbit ETH				SGMII	USB	4x GTR on G2	
TE0821*	B26	48	HD	VC CIOA	B65	16	HP	VC CIOB	B65	18	HP	VC CIOB	B24	48	HD	VC CIOD	B5	6	MIO	3.3 V	B5 01	8	MIO	3.3 V	1x Gbit ETH				SGMII	USB	4x GTR on G2	
TE0823*	B66	48	HP	VC CIOA	B65	16	HP	VC CIOB	B65	18	HP	VC CIOB	B64	50	HP	VC CIOD	B5	6	MIO	3.3 V	B5 01	8	MIO	3.3 V	1x Gbit ETH				SGMII	USB	4x GTR on G2	
TE0741	B13	48	HR	VC CIOA	B16	16	HR	VC CIOB	B15	18	HR	VC CIOB	B12	50	HR	VC CIOD	1x GTX	1 Lane					B14	8	HR	3.3 V	2x GTX	2 Lan es		1x GTX		4x GTX on G2
TE0742*																																
TE0841	B64	48	HR	VC CIOA	B66	16	HP	VC CIOB	B68	18	HP	VC CIOB	B67	50	HP	VC CIOD	1x GTH	1 Lane					B65	8	HR	3.3 V	2x GTH	2 Lan es		1x GTH		4x GTH on G2
TE0842*																																

I/O resource comparison for all 4x5 modules. There are maximum 4 user supplied I/O voltages (VCCIOA, VCCIOB, VCCIOC and VCCIOD).

*Attention: Maximum supply voltage for HP banks is 1.8V.

Module B2B FPGA-Banks and Voltages

Module Pinout Overview

Direction		Name	Pin	Name	Pin	Direction
in/out	MGT TX	ETH SOUT	GROUP1	1	2	MGT FN [ETH S]M GROUP8
in/out	MGT TX	ETH SOUT	GROUP1	3	4	MGT FN [ETH S]M GROUP8
in/out	MGT TX	ETH SOUT	GROUP1	5	6	MGT FN [ETH S]M GROUP8
in/out	MGT TX	ETH SOUT	GROUP1	7	8	MGT FN [ETH S]M GROUP8
in/out	MGT TX	ETH SOUT	GROUP1	9	10	MGT FN [ETH S]M GROUP8
in/out	MGT TX	ETH SOUT	GROUP1	11	12	MGT FN [ETH S]M GROUP8
in/out	MGT TX	ETH SOUT	GROUP1	13	14	MGT FN [ETH S]M GROUP8
in/out	MGT TX	ETH SOUT	GROUP1	15	16	MGT FN [ETH S]M GROUP8
in/out	MGT TX	ETH SOUT	GROUP1	17	18	MGT FN [ETH S]M GROUP8
in/out	MGT TX	ETH SOUT	GROUP1	19	20	MGT FN [ETH S]M GROUP8
in/out	MGT TX	ETH SOUT	GROUP1	21	22	MGT FN [ETH S]M GROUP8
in/out	MGT TX	ETH SOUT	GROUP1	23	24	MGT FN [ETH S]M GROUP8
in/out	MGT TX	ETH SOUT	GROUP1	25	26	MGT FN [ETH S]M GROUP8
in/out	MGT TX	ETH SOUT	GROUP1	27	28	MGT FN [ETH S]M GROUP8
in/out	MGT TX	ETH SOUT	GROUP1	29	30	MGT FN [ETH S]M GROUP8
in/out	MGT TX	ETH SOUT	GROUP1	31	32	MGT FN [ETH S]M GROUP8
in/out	MGT TX	ETH SOUT	GROUP1	33	34	MGT FN [ETH S]M GROUP8
in/out	MGT TX	ETH SOUT	GROUP1	35	36	MGT FN [ETH S]M GROUP8
in/out	MGT TX	ETH SOUT	GROUP1	37	38	MGT FN [ETH S]M GROUP8
in/out	MGT TX	ETH SOUT	GROUP1	39	40	MGT FN [ETH S]M GROUP8
in/out	MGT TX	ETH SOUT	GROUP1	41	42	MGT FN [ETH S]M GROUP8
in/out	MGT TX	ETH SOUT	GROUP1	43	44	MGT FN [ETH S]M GROUP8
in/out	MGT TX	ETH SOUT	GROUP1	45	46	MGT FN [ETH S]M GROUP8
in/out	MGT TX	ETH SOUT	GROUP1	47	48	MGT FN [ETH S]M GROUP8
in/out	MGT TX	ETH SOUT	GROUP1	49	50	MGT FN [ETH S]M GROUP8
in/out	MGT TX	ETH SOUT	GROUP1	51	52	MGT FN [ETH S]M GROUP8
in/out	MGT TX	ETH SOUT	GROUP1	53	54	MGT FN [ETH S]M GROUP8
in/out	MGT TX	ETH SOUT	GROUP1	55	56	MGT FN [ETH S]M GROUP8
in/out	MGT TX	ETH SOUT	GROUP1	57	58	MGT FN [ETH S]M GROUP8
in/out	MGT TX	ETH SOUT	GROUP1	59	60	MGT FN [ETH S]M GROUP8
in/out	MGT TX	ETH SOUT	GROUP1	61	62	MGT FN [ETH S]M GROUP8
in/out	MGT TX	ETH SOUT	GROUP1	63	64	MGT FN [ETH S]M GROUP8
in/out	MGT TX	ETH SOUT	GROUP1	65	66	MGT FN [ETH S]M GROUP8
in/out	MGT TX	ETH SOUT	GROUP1	67	68	MGT FN [ETH S]M GROUP8
in/out	MGT TX	ETH SOUT	GROUP1	69	70	MGT FN [ETH S]M GROUP8
in/out	MGT TX	ETH SOUT	GROUP1	71	72	MGT FN [ETH S]M GROUP8
in/out	MGT TX	ETH SOUT	GROUP1	73	74	MGT FN [ETH S]M GROUP8
in/out	MGT TX	ETH SOUT	GROUP1	75	76	MGT FN [ETH S]M GROUP8
in/out	MGT TX	ETH SOUT	GROUP1	77	78	MGT FN [ETH S]M GROUP8
in/out	MGT TX	ETH SOUT	GROUP1	79	80	MGT FN [ETH S]M GROUP8
in/out	MGT TX	ETH SOUT	GROUP1	81	82	MGT FN [ETH S]M GROUP8
in/out	MGT TX	ETH SOUT	GROUP1	83	84	MGT FN [ETH S]M GROUP8
in/out	MGT TX	ETH SOUT	GROUP1	85	86	MGT FN [ETH S]M GROUP8
in/out	MGT TX	ETH SOUT	GROUP1	87	88	MGT FN [ETH S]M GROUP8
in/out	MGT TX	ETH SOUT	GROUP1	89	90	MGT FN [ETH S]M GROUP8
in/out	MGT TX	ETH SOUT	GROUP1	91	92	MGT FN [ETH S]M GROUP8
in/out	MGT TX	ETH SOUT	GROUP1	93	94	MGT FN [ETH S]M GROUP8
in/out	MGT TX	ETH SOUT	GROUP1	95	96	MGT FN [ETH S]M GROUP8
in/out	MGT TX	ETH SOUT	GROUP1	97	98	MGT FN [ETH S]M GROUP8
in/out	MGT TX	ETH SOUT	GROUP1	99	100	MGT FN [ETH S]M GROUP8

Direction	Name	Pin	Name	Pin	Direction
in	PWR_1	1	GND	2	
in	PWR_1	3	GROUP2	4	ETH MDIOD
in	PWR_1	5	GROUP1	6	ETH MDIOD
in	NOSE0	7	8	MGT FN	GROUP2
in	VCCIOA	9	10	GROUP1	ETH MDIOD
in	VCCIOA	11	12	GROUP1	ETH MDIOD
in	PWR_2	13	14	ETH_S0E	
in	PWR_2	15	16	GROUP1	ETH MDIOD
in/out	GROUP5	MIO	SD D3	MGT TX	17
in/out	GROUP5	MIO	SD D2	MGT TX	19
in/out	GROUP5	MIO	SD D1	GND	21
in/out	GROUP5	MIO	SD D0	GND	23
in/out	GROUP5	MIO	SD CMD	MGT RX	25
in/out	GROUP5	MIO	SD CLK	MGT RX	27
in	GND	29	30	SC_TN1	
in	GROUP1	31	32	SC_BOOTMODE	
in	GROUP1	33	34	GROUP1	
in	GROUP1	35	36	GROUP1	
in	GROUP1	37	38	GROUP1	
in	GROUP1	39	40	GROUP1	
in	GROUP1	41	42	GROUP1	
in	GROUP1	43	44	GROUP1	
in	GROUP1	45	46	GROUP1	
in	GROUP1	47	48	GROUP1	
in	GROUP1	49	50	GROUP1	
in	GROUP1	51	52	GROUP1	
in	GND	53	54	GND	
in	GROUP1	55	56	GROUP1	
in	GROUP1	57	58	GROUP1	
in	GROUP1	59	60	GROUP1	
in	GROUP1	61	62	GROUP1	
in	GROUP1	63	64	GROUP1	
in	GROUP1	65	66	GROUP1	
in	GROUP1	67	68	GROUP1	
in	GROUP1	69	70	GROUP1	
in	GROUP1	71	72	GROUP1	
in	GROUP1	73	74	GROUP1	
in	GROUP1	75	76	GROUP1	
in	GROUP1	77	78	GROUP1	
in	GROUP1	79	80	GROUP1	
in	GROUP1	81	82	GROUP1	
in	GROUP1	83	84	GROUP1	
in/out	GROUP5	MIO	UART TX	85	
in/out	GROUP5	MIO	UART RX	87	
in	GROUP1	JTAG_SLL	89	90	
in/out	GROUP6	MIO	GROUP5	MIO	UART RX
in/out	GROUP6	MIO	93	94	GROUP1
in/out	GROUP6	MIO	95	96	GROUP1
in/out	GROUP6	MIO	97	98	GROUP1
in/out	GROUP6	MIO	99	100	GROUP1

Positions are displayed as Top View

Legend
Power-VCC
Power-GND
GROUP1
GROUP2
GROUP3
GROUP4
GROUP5
GROUP6
GROUP7
GROUP8
GROUP9
Special
VCCIOA
VCCIOB
VCCIOC
VCCIOD

Direction	Name	Pin	Name	Pin	Direction
in	VCCIOB	1	2	PWR_1	in
in	VCCIOB	3	4	PWR_1	in
in	VCCIOC	5	6	PWR_1	in
in	VCCIOD	7	8	PWR_1	in
in	GROUP3	9	10	PWR_1M1	out
in	GROUP3	11	12	PWR_1M1	out
in	GROUP3	13	14	GROUP3	io
in	GROUP3	15	16	GROUP3	io
in	GROUP3	17	18	SC_AKST	io
in	PWR_1M1M1	19	20	GND	
in	GROUP3	21	22	GROUP3	io
in	GROUP3	23	24	GROUP3	io
in	GROUP3	25	26	GROUP3	io
in	GROUP3	27	28	GROUP3	io
in	GROUP3	29	30	GROUP3	io
in	GROUP3	31	32	GROUP4	io
in	GROUP3	33	34	GROUP4	io
in	GROUP3	35	36	GROUP4	io
in	GROUP3	37	38	GROUP4	io
in	GROUP3	39	40	GROUP4	io
in	GROUP4	41	42	GROUP4	io
in	GROUP4	43	44	GROUP4	io
in	GROUP4	45	46	GROUP4	io
in	GROUP4	47	48	GROUP4	io
in	GROUP4	49	50	GROUP4	io
in	GROUP4	51	52	GROUP4	io
in	GROUP4	53	54	GROUP4	io
in	GROUP4	55	56	GROUP4	io
in	GROUP4	57	58	GROUP4	io
in	GND	59	60	GND	
in	GROUP4	61	62	GROUP4	io
in	GROUP4	63	64	GROUP4	io
in	GROUP4	65	66	GROUP4	io
in	GROUP4	67	68	GROUP4	io
in	GROUP4	69	70	GROUP4	io
in	GROUP4	71	72	GROUP4	io
in	GROUP4	73	74	GROUP4	io
in	GROUP4	75	76	GROUP4	io
in	GROUP4	77	78	GROUP4	io
in	GROUP4	79	80	GROUP4	io
in	GROUP4	81	82	GROUP4	io
in	GROUP4	83	84	GROUP4	io
in	GROUP4	85	86	GROUP4	io
in	GROUP4	87	88	GROUP4	io
in	GROUP4	89	90	GROUP4	io
in	PWR_1M1M1	91	92	GROUP4	io
in	TMS	93	94	GROUP4	io
in	TDI	95	96	GROUP4	io
out	TDO	97	98	GROUP4	io
in	TCX	99	100	GROUP4	io

Module basic power and group pin assignment, recommended to verify with Schematics

Carrier Board Power Connection Table

IO Voltage	B2B Connector	Carrier Boards																	
		Name	Direction*	JB1	JB2	TE0701		TE0703 Rev01 - Rev04		TE0703 Rev 05		TE0705		TE0706		TEBA0841		TEBA0841 REV01	
		Pin	Pin	Schematic Name	Value, Option, Comp.	Schematic Name	Value, Option, Comp.	Schematic Name	Value, Option, Comp.	Schematic Name	Value, Option, Comp.	Schematic Name	Value, Option, Comp.	Schematic Name	Value, Option, Comp.	Schematic Name	Value, Option, Comp.	Schematic Name	Value, Option, Comp.
PWR_1	out	2,4,6	1,3,5,7	5V0	5V	3.3V	3.3V	3.3V	3.3V	3.3V	3.3V	3.3V	3.3V	3.3V	3.3V	3.3V	use ext. 3.3V power supply	3.3V	use ext. 3.3V power supply
VCCIOA	out	10,12		VIOTB	FMC_VA DJ 2V5 3.3VOUT	VCCIO35	R23M3.3VOUT J1B-B1	VCCIOA	J5M3.3VOUT, M1.8VOUT R23M3.3VOUT J1-B1	VIOTB	FMC_VA DJ 2V5 3.3VOUT	VCCIO35	R20->M3.3VOUT/J6B-B32	VCCIOA	J26 M1.8VOUT, 2.5V, 3.3V_OUT J20-6, J20-45	VCCIOA	J26 M1.8VOUT, 2.5V, 3.3V_OUT J20-6, J20-45		

VCCIOD	out		8,10	VIOTB	FMC_VA DJ 2V5 3.3VOUT	VCCIO13	R26M3. 3VOUT J2B-B1	VCCIOD	J10M3. 3VOUT, M1. 8VOUT R26M3. 3VOUT J2B-B1	VIOTB	FMC_VA DJ 2V5 3.3VOUT	VCCIO13	R22->M3. 3VOUT/J6B- B1	VCCIOD	J27 M1.8VOUT, 2.5V, 3.3V_OUT J17-6,J17-45	VCCIOD	J27 M1.8VOUT, 2.5V, 3.3V_OUT J17-6,J17-45
PWR_2	out	14,16		3V3IN	3.3V	3.3V	3.3V	3.3V	3.3V	3V3IN	3.3V	3.3V	3.3V	3.3V	use ext. 3.3V power supply	3.3V	use ext. 3.3V power supply
VCCIOB	out		2,4	no name / VIOTA	FMC_VA DJ 2V5 3.3VOUT	VCCIO34	J5M3. 3VOUT J1B-B32	VCCIOB	J8M3.3VOUT, M1.8VOUT J2B-B32	VIOTB	FMC_VA DJ 2V5 3.3VOUT	1.8V	1.8V	VCCIOB	J5 M1.8VOUT, 2.5V, 3.3V_OUT	VCCIOB	NC
VCCIOC	out		6	no name / VIOTA	FMC_VA DJ 2V5 3.3VOUT	VCCIO33	R25M3. 3VOUT J2B-B32	VCCIOC	J9M3. 3VOUT, M1. 8VOUT R25M3. 3VOUT J2B-B32	VIOTB	FMC_VA DJ 2V5 3.3VOUT	VCCIO33	R21->M3. 3VOUT	VCCIOC	J6 M1.8VOUT, 2.5V, 3.3V_OUT	VCCIOC	NC
PWR_M1	in		9,11	3.3 VOUT	3.3V	3.3 VOUT	3.3V	M3. 3VOUT	3.3V	3.3 VOUT	3.3V	M3. 3VOUT	3.3V	3.3 V_OUT	3.3V	3.3 V_OUT	3.3V
PWR_M2	in	40		VI0B	1.8V	M1. 8VOUT	1.8V	M1. 8VOUT	1.8V	VI0B	1.8V	M1. 8VOUT	1.8V	M1. 8VOUT	1.8V	M1. 8VOUT	1.8V
PWR_M3	in		20	NC		NC		NC		NC		NC		NC		NC	NC
PWR_VBAT	out	80		VBAT	B1	VBAT	J7	VBAT	J7	NC		VBAT	J9	VBAT	NC	VBAT	NC
PWR_JTAG	in		92	VCCJTAG		VCCJTAG		VCCJTAG		VCCJTAG		VCCJTAG		VCCJTAG		VCCJTAG	NC

Power comparison of all 4x5 carrier boards. ***Power direction based on carrier boards view.** There are 4 variable user supplied I/O voltages (VCCIOA, VCCIOB, VCCIOC and VCCIOD). PWR_1 and PWR_2 are fixed from carrier boards. PWR_M1 and PWR_M2 normally use default value from module. NC=Not Connected

Attention: On some carrier boards the user supplied I/O voltages are connected together (red colored schematic names).

Power Pin Connection on different Carrierboards

Carrier Pinout Overview

JB1					JB2						
Direction	Name	Pin	Pin	Direction	Direction	Name	Pin	Pin	Direction		
out	PWR_1	2	1	GND	out	VCCIOB	2	1	PWR_1	out	
out	PWR_1	4	3	ID	out	VCCIOB	4	3	PWR_1	out	
out	PWR_1	6	5	ID	out	VCCIOE	8	5	PWR_1	out	
io	NOSEQ	8	7	GND	out	VCCIOD	8	7	PWR_1	out	
out	VCCIOA	10	9	ID	out	VCCIOB	10	9	PWR_M1	in	
out	VCCIOA	12	11	ID	out	VCCIOB	12	11	PWR_M1	in	
out	PWR_2	14	13	ETH_VCC	ID	ID	14	13	ID		
out	PWR_2	16	15	ID	ID	ID	16	15	ID		
ID	ID	18	17	ID	ID	ID	18	17	SC_nRST	out	
ID	ID	20	19	GND	out	PWR_M1nAC	20	19	GND		
ID	ID	22	21	ID	ID	ID	22	21	ID		
ID	ID	24	23	ID	ID	ID	24	23	ID		
ID	ID	26	25	GND	ID	ID	26	25	ID		
ID	ID	28	27	SC_EN1	out	ID	28	27	ID		
GND	GND	30	29	SC_PG00D	io	IO/GND	30	29	GND		
ID	ID	32	31	SC_BOOTMODE	out	ID	32	31	ID		
ID	ID	34	33	ID	ID	ID	34	33	ID		
ID	ID	36	35	ID	ID	ID	36	35	ID		
ID	ID	38	37	ID	ID	ID	38	37	ID		
in	PWR_M1	40	39	ID	ID	IO	40	39	GND		
ID	ID	42	41	ID	ID	ID / Special	42	41	ID		
ID	ID	44	43	GND	ID	VCCIOA	44	43	ID		
ID	ID	46	45	ID	ID	VCCIOA	46	45	ID		
ID	ID	48	47	ID	ID	VCCIOA	48	47	ID		
ID	ID	50	49	ID	ID	GND	50	49	GND		
ID	ID	52	51	ID	ID	ID	52	51	ID		
GND	GND	54	53	GND	ID	ID	54	53	ID		
ID	ID	56	55	ID	ID	ID	56	55	ID		
ID	ID	58	57	ID	ID	ID	58	57	ID		
ID	ID	60	59	ID	ID	GND	60	59	GND		
ID	ID	62	61	ID	ID	ID	62	61	ID		
GND	GND	64	63	GND	ID	ID	64	63	ID		
ID	ID	66	65	ID	ID	ID	66	65	ID		
ID	ID	68	67	ID	ID	ID	68	67	ID		
ID	ID	70	69	ID	ID	GND	70	69	GND		
GND	GND	74	73	GND	ID	ID	74	73	ID		
ID	ID	76	75	ID	ID	ID	76	75	ID		
ID	ID	78	77	ID	ID	ID	78	77	ID		
out	PWR_M1n	80	79	ID	ID	GND	80	79	GND		
ID	ID	82	81	ID	ID	ID	82	81	ID		
ID	ID	84	83	GND	ID	ID	84	83	ID		
in	IO/UART TX	86	85	ID	ID	ID	86	85	ID		
ID	ID	88	87	ID	ID	ID	88	87	ID		
out	JTAGSEL	90	89	GND	in	IO	90	89	GND		
ID	ID	92	91	IO/UART RX	out	in	PWR_M1n	92	91	ID	
ID	ID	94	93	ID	ID	out	TMS	94	93	ID	
ID	ID	96	95	ID	ID	out	TDI	96	95	ID	
ID	ID	98	97	ID	ID	in	TDO	98	97	ID	
ID	ID	100	99	ID	ID	out	TCK	100	99	ID	

Positions are displayed as Top View

Legend	
Red	Power VCC
Light Blue	Power-GND
Dark Blue	Special IO
Light Green	ID / Special
Yellow	VCCIOA
Light Purple	VCCIOE
Light Orange	VCCIOD

Carrierboard basic power and group pin assignment (Top View), recommended to verify with Schematics

4x5 Module Controller IOs

Name	Module B2B Pin	Carrier B2B Pin	Direction (Module view)	Description	Recommendation
JTAGSEL	JM1-89	JB1-90	in	JTAG Chain multiplexer. Low FPGA, High CPLD. For module with CPLD only.	Connect Pulldown on carrier. DIP switch possible.
SC_EN1	JM1-28	JB1-27	in	Module power. Set high to enable module power. Note: Power management depends on module. Sometimes this is a only used as Power ON Reset like SC_nRST	Connect Pullup on carrier. DIP switch possible
SC_NO SEQ	JM1-7	JB1-8	in / inout	Module Power management. Set high to disable CPLD power management. Note: Power management depends on module and not all modules support extended power management with CPLD.	Connect Pullup or force to GND over zero ohm resistor on carrier. DIP switch possible.
SC_PG OOD	JM1-30	JB1-29	out / inout	Power Good signal. Is Low, if SC_EN1 is set to zero or if power is not ready, otherwise high impedance output. Note: Power management depends on module.	Connect Pullup on carrier. Do not use this signal to enable FPGA Bank voltages. It's only for monitoring. To Enable FPGA Banks, use 3.3V(PWR_M1) or 1.8V(PWR_M2) module output.

SC_BO OTMODE	JM1-32	JB1-31	in	Boot Mode selection Pin for Zynq module only. Default low for primary SD boot and high for primary QSPI boot. Note: Depends also on module CPLD firmware	Connect Pullup on carrier. DIP switch possible.
SC_nRST	JM2-18	JB2-17	in	Low active module reset. Pin force Power one reset on FPGA /SoC. Note: Depending from module CPLD or voltage supervisor is used.	Connect Pullup on carrier. DIP switch possible.



It's planned to use SC_PGOOD of also additional Boot Mode Pin (Pin is bidirectional, pull up or force to zero), to additionally set JTAG only boot mode (to avoid programming problems with some vivado versions, see: [AR#00002 - QSPI Programming issues](#))

4x5 Module Controller IOs

Remove 4x5 module



Always loosen the screws only a little step by step so that the module is evenly squeezed out. Otherwise solder contacts can break.

Compatibility Guide

Ethernet LED'S

TE07xx 4x5 modules do not have dedicated pins for the Ethernet PHY LED's, also there are no fix pins on the baseboards for the PHY LED's or any other LED's.

If Ethernet JACKs on Baseboard have LED's then those should be connected to some free PL I/O pins, and then routed in the FPGA logic from the PHY to the I/O Pin in the B2B Connector.

Recommended connections would be to use JM2.89 and JM2.100 for the PHY LED's, those positions support baseboard ETH LED's for TE0701 and TE0703 and TE0706.

JM2 pins 1, 3 (TE0720 Bank 34 Voltage)

To be compatible with TE0720 JM2 pins 1,3 must be connected to some valid VCCIO voltage.

When JM2 pins 1, 3 are not powered TE0720 would not boot, and may not be recognized in JTAG chain as well.

When those pins are not used on the module (TE0710) then to be compatible with TE0720:

Solution A: connect to 3.3V out from the module, option compatible to all modules except those with HP banks (TE0715-01-30)

Solution B: connect to 1.8V out from the module, option compatible with all modules.

Carrier Board Checklist

Schematic Checklist

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1	Are B2B pin numbers on the connectors mirrored compared to the module pin numbers?	As B2B connectors are "unisex" type they do mirror pin numbers when connecting. That is pin1 connects to pin2, and pin2 to pin1, etc.
2	Are B2B connectors named JB1, JB2, JB3?	This is not a hard requirement, but it helps to use the same identifiers.
3	Are all GND pins connected to a common ground net?	
4	Are all VIN pins connected together?	
5	Is JB2 pin 92 pin used as VREF for the JTAG interface?	for future compatibility only, currently all modules have 3.3V JTAG
6	For 7 Series Zynq module only: Are external circuits/buffers connecting to MIO bank 1 pins powered from JB1 pin 40?	JB1 pins 18, 20, 22, 24, 26, 28 use voltage at pin 40 as VCCIO. Currently it is 1.8V for 4x5 Zynq Modules. Note: Different Power supply on TE0820(3.3V MIO Bank) and normal FPGA modules(check schematics)

PCB Checklist

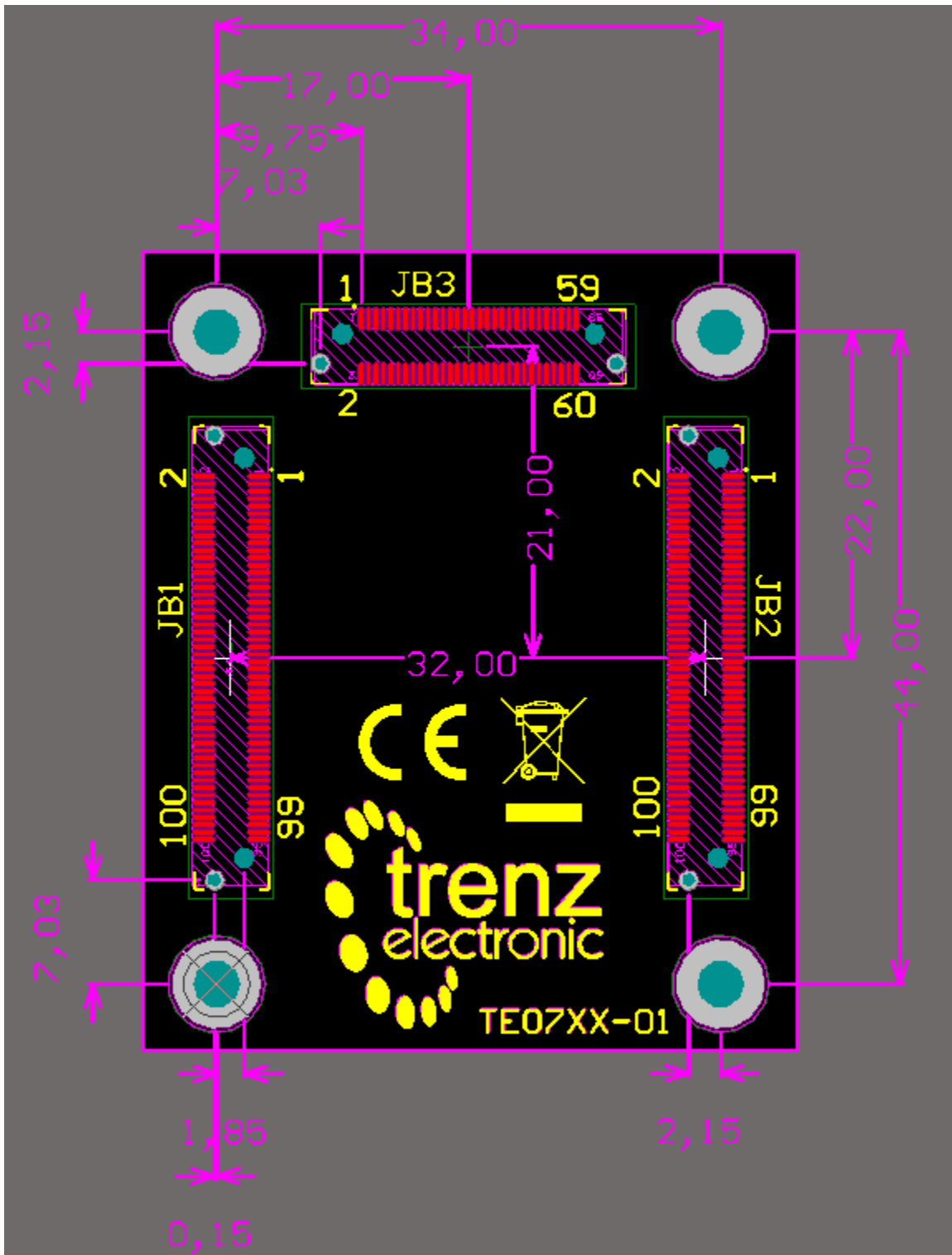
1	Are mounting holes placed properly?	Four Mounting holes should always be used. They are required for mounting screws and for module extraction. The mounting holes will also help in dissipating some heat from the module to the carried board PCB. Four holes with a 3.2mm diameter should be placed exactly at the corners of a 34mm by 44mm rectangle.
2	Are B2B headers properly placed?	B2B headers must be placed and aligned very precisely or the module will not align correctly (in the worst case module insertion could destroy the connectors or the PCB). The B2B headers should be locked on the PCB, and it is recommended that the position and placement be checked against placement dimensions before submitting the PCB files.
3	Are B2B headers rotated properly?	As B2B header pin numbers differ from module to the carrier (swap of odd and even numbers), it is recommended that the rotation is checked in the PCB design.
4	Height clearance below module	Components can be placed below the module but height clearance rules must be obeyed.
5	Power dissipation of components below module	It is not recommended to place any components with high power dissipation below the module, as there will be almost no airflow below the module.

Visual Check of Module placement

It is highly recommended to use the Base board Template designs as a starting point for new PCB designs. If that is not possible, then adding linear dimensions in the design helps to check that all connectors and mounting holes are properly placed.



This placement is same for all 4x5 Modules!



Top view of the Carrier Board.

Connector numbers as on base! (pin JB1.1 on base would mate to pin JM1.2 on module).