TE0711 Test Board

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Overview

Simple MicroBlaze Design with Hello TE0711 and LED control via VIO. Refer to http://trenz.org/te0711-info for the current online version of this manual and other available documentation.

Key Features

- Vitis/Vivado 2019.2
- MicroBlaze
- LED
- QSPI

- UART

Revision History

Date	Vivado	Project Built	Authors	Description
2020-09-01	2019.2	TE0711-test_board-vivado_2019.2-build_14_20200901073500.zip TE0711-test_board_noprebuilt-vivado_2019.2-build_14_20200901073630.zip	John Hartfiel	• 2019.2 update
2017-12-07	2017.2	TE0711-test_board_noprebuilt-vivado_2017.2-build_05_20171207122944.zip TE0711-test_board-vivado_2017.2-build_05_20171207122644.zip	John Hartfiel	• initial release

Design Revision History

Release Notes and Know Issues

Issues	Description	Workaround	To be fixed version
No known issues	---	---	---

Known Issues

Requirements

Software

Software	Version	Note
Vitis	2019.2	needed, Vivado is included into Vitis installation

Software

Hardware

Basic description of TE Board Part Files is available on TE Board Part Files.

Complete List is available on <design name>/board_files/*_board_files.csv

Design supports following modules:

Module Model	Board Part Short Name	PCB Revision Support	DDR	QSPI Flash	EMMC	Others	Notes
TE0711-01-35-2C	35_2c	REV01	NA	32MB	NA	NA	NA
TE0711-01-100-2C	100_2c	REV01	NA	32MB	NA	NA	NA
TE0711-01-35-2I	35_2i	REV01	NA	32MB	NA	NA	NA
TE0711-01-100-2I	100_2i	REV01	NA	32MB	NA	NA	NA

Hardware Modules

Design supports following carriers:

Carrier Model	Notes

TE0701	• See restrictions on usage with 7 Series Carriers: 4 x 5 SoM Carriers
TE0703	• See restrictions on usage with 7 Series Carriers: 4 x 5 SoM Carriers • Used as reference carrier.
TE0705	• See restrictions on usage with 7 Series Carriers: 4 x 5 SoM Carriers
TE0706	• See restrictions on usage with 7 Series Carriers: 4 x 5 SoM Carriers
TEBA0841	• See restrictions on usage with 7 Series Carriers: 4 x 5 SoM Carriers • No SD Slot available, pins goes to Pin Header

Hardware Carrier

Additional HW Requirements:

Additional Hardware	Notes
USB Cable for JTAG/UART	Check Carrier Board and Programmer for correct typ
XMOD Programmer	Carrier Board dependent, only if carrier has no own FTDI

Additional Hardware

Content

For general structure and of the reference design, see Project Delivery - Xilinx devices

Design Sources

Type	Location	Notes
Vivado	<design name>/block_design <design name>/constraints <design name>/ip_lib	Vivado Project will be generated by TE Scripts
Vitis	<design name>/sw_lib	Additional Software Template for Vitis and apps_list.csv with settings automatically for Vitis app generation

Design sources

Additional Sources

Type	Location	Notes
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Additional design sources

Prebuilt

File	File-Extension	Description
BIT-File	*.bit	FPGA (PL Part) Configuration File
DebugProbes-File	*.ltx	Definition File for Vivado/Vivado Labtools Debugging Interface
Diverse Reports	---	Report files in different formats
Hardware-Platform-Specification-Files	*.xsa	Exported Vivado Hardware Specification for Vitis and PetaLinux
LabTools Project-File	*.lpr	Vivado Labtools Project File
MCS-File	*.mcs	Flash Configuration File with Boot-Image (MicroBlaze or FPGA part only)
MMI-File	*.mmi	File with BRAM-Location to generate MCS or BIT-File with *.elf content (MicroBlaze only)
Software-Application-File	*.elf	Software Application for Zynq or MicroBlaze Processor Systems

Prebuilt files (only on ZIP with prebult content)

Download

Reference Design is only usable with the specified Vivado/SDK/PetaLinux/SDx version. Do never use different Versions of Xilinx Software for the same Project.

Reference Design is available on:

- TE0711 "Test Board" Reference Design Download Area

Design Flow

Reference Design is available with and without prebuilt files. It's recommended to use TE prebuilt files for first lunch.

Trenz Electronic provides a tcl based built environment based on Xilinx Design Flow.

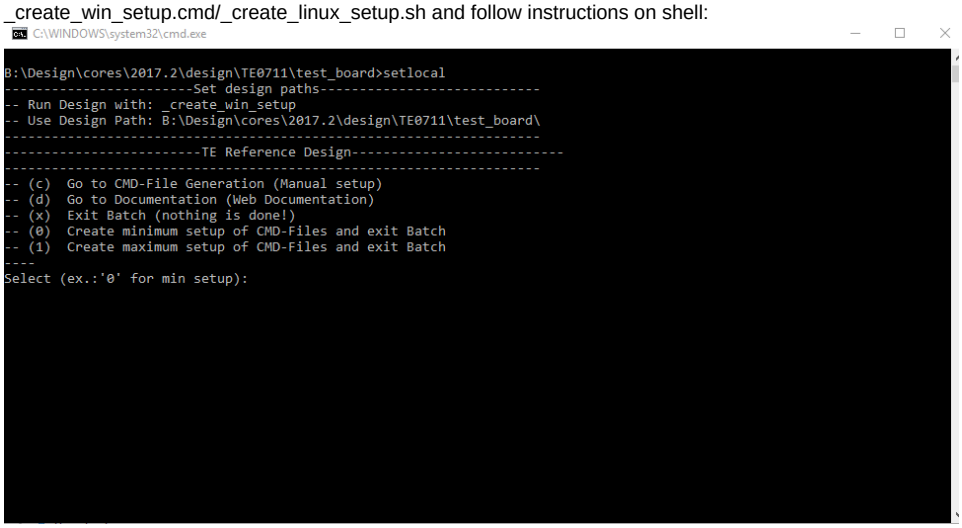
See also:

- Xilinx Development Tools#XilinxSoftware-BasicUserGuides
- Vivado Projects - TE Reference Design
- Project Delivery.

The Trenz Electronic FPGA Reference Designs are TCL-script based project. Command files for execution will be generated with "_create_win_setup.cmd" on Windows OS and "_create_linux_setup.sh" on Linux OS.

TE Scripts are only needed to generate the vivado project, all other additional steps are optional and can also executed by Xilinx Vivado/SDK GUI. For currently Scripts limitations on Win and Linux OS see: Project Delivery Currently limitations of functionality

1. _create_win_setup.cmd/_create_linux_setup.sh and follow instructions on shell:



2. Press 0 and enter to start "Module Selection Guide"
3. (optional Win OS) Generate Virtual Drive or use short directory for the reference design (for example x:\<design name>)
4. Create Project (follow instruction of the product selection guide), settings file will be configured automatically during this process)
    a. (optional for manual changes) Select correct device and Xilinx install path on "design_basic_settings.cmd" and create Vivado project with "vivado_create_project_guimode.cmd"
    Note: Select correct one, see alsoTE Board Part Files
5. Create XSA and export to prebuilt folder
    a. Run on Vivado TCL: TE::hw_build_design -export_prebuilt
    Note: Script generate design and export files into \prebuilt\hardware\<short dir>. Use GUI is the same, except file export to prebuilt folder
6. Generate ApplicationFiles with Vitis
    a. Run on Vivado TCL: TE::sw_run_vitis -all
    Note: Scripts generate applications and bootable files, which are defined in "sw_lib\apps_list.csv"
    b. (alternative) Start SDK with Vivado GUI or start with TE Scripts on Vivado TCL: TE::sw_run_vitis
    Note: TCL scripts generate also platform project, this must be done manuelly in case GUI is used. See Vitis
7. Copy Application (hello_te0711.elf) into \firmware\microblaze_0\
8. Regenerate Design:
    a. Run on Vivado TCL: TE::hw_build_design -export_prebuilt
    Note: App from Firmware folder will be add into BlockRAM. If you add other app, you must select *.elf manually on Vivado
    b. (alternative) Use SDK or Vivado to update generate Bitfile with new Application and regenerate mcs manually.

Launch

Programming

⚠ Check Module and Carrier TRMs for proper HW configuration before you try any design.

Xilinx documentation for programming and debugging: Vivado/SDK/SDSoC-Xilinx Software Programming and Debugging

Get prebuilt boot binaries

1. _create_win_setup.cmd/_create_linux_setup.sh and follow instructions on shell
2. Press 0 and enter to start "Module Selection Guide"
    a. Select assembly version
    b. Validate selection
    c. Select Create and open delivery binary folder
    Note: Folder (<project foler>/_binaries_<Artikel Name>) with subfolder (boot_<app name>) for different applications will be generated

QSPI

Optional for Boot.bin on QSPI Flash and image.ub on SD.

1. Connect JTAG and power on carrier with module
2. Open Vivado Project with "vivado_open_existing_project_guimode.cmd" or if not created, create with "vivado_create_project_guimode.cmd"
3. Type on Vivado TCL Console: TE::pr_program_flash -swapp hello_te0711
4. Reboot (if not done automatically)

SD

Not used on this Example.

JTAG

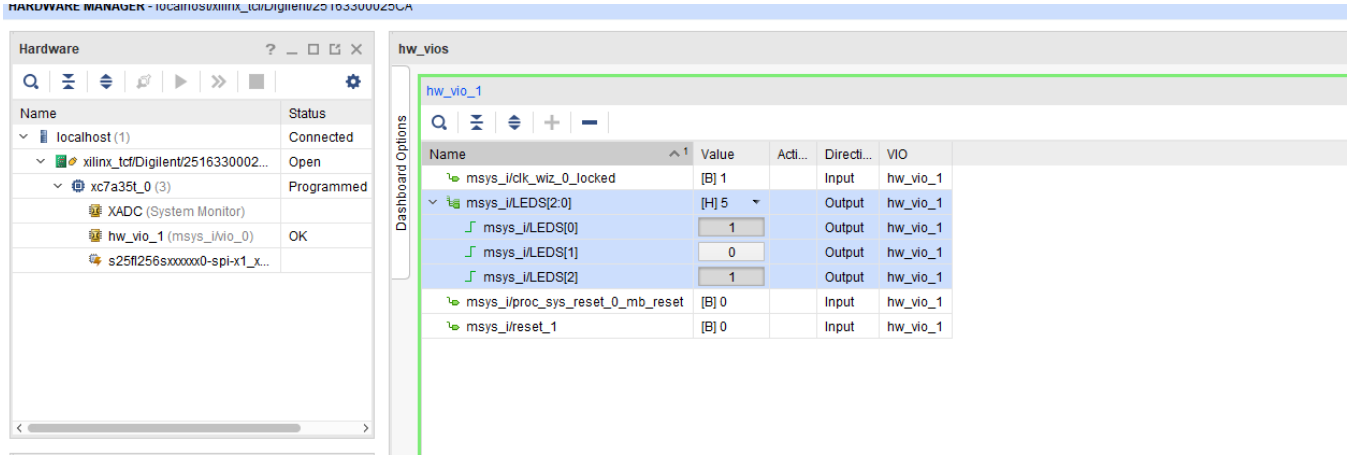
- Open Vivado HW Manager with
- Program FPGA with Bitstream

Usage

1. Prepare HW like described on section TE0711 Test Board#Programming
2. Connect UART USB (most cases same as JTAG)
3. Power On PCB
   Note: FPGA Loads Bitfile from Flash

Vivado HW Manager

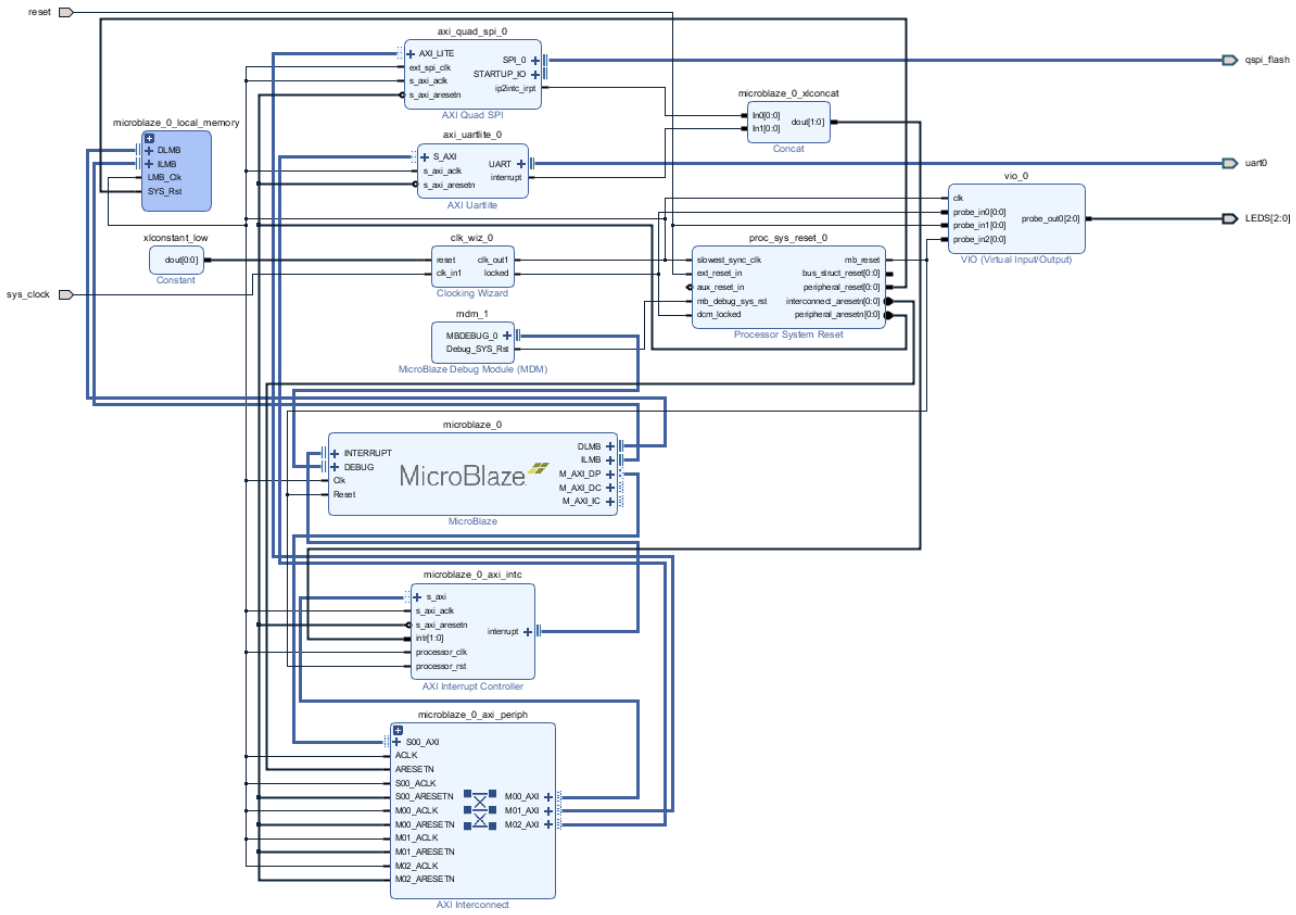
1. Open Vivado HW-Manager and add VIO signal to dashboard (*.ltx located on prebuilt folder)
    a. Select LEDs and set to Toggle Button
       Note: LEDS[0]=D1, LEDS[1]=D2,LEDS[2=D3 on PCB. LEDS[2] is inverted on PCB.



Vivado Hardware Manager

System Design - Vivado

Block Design



Block Design

Constrains

Basic module constrains

_i_bitgen_common.xdc

```
set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design]
set_property BITSTREAM.CONFIG.CONFIGRATE 66 [current_design]
set_property CONFIG_VOLTAGE 3.3 [current_design]
set_property CFGBVS VCCO [current_design]
set_property CONFIG_MODE SPIx4 [current_design]
set_property BITSTREAM.CONFIG.SPI_32BIT_ADDR YES [current_design]
set_property BITSTREAM.CONFIG.SPI_BUSWIDTH 4 [current_design]
set_property BITSTREAM.CONFIG.M1PIN PULLNONE [current_design]
set_property BITSTREAM.CONFIG.M2PIN PULLNONE [current_design]
```

```
set_property BITSTREAM.CONFIG.M0PIN PULLNONE [current_design]

set_property BITSTREAM.CONFIG.USR_ACCESS TIMESTAMP [current_design]
```

_i_bitgen.xdc

```
set_property BITSTREAM.CONFIG.UNUSEDPIN PULLDOWN [current_design]
```

Design specific constrain

_i_io.xdc

```
set_property PACKAGE_PIN A8 [get_ports {LEDS[0]}]
set_property PACKAGE_PIN L15 [get_ports {LEDS[1]}]
set_property PACKAGE_PIN R17 [get_ports {LEDS[2]}]
set_property IOSTANDARD LVCMOS18 [get_ports {LEDS[0]}]
set_property IOSTANDARD LVCMOS33 [get_ports {LEDS[1]}]
set_property IOSTANDARD LVCMOS33 [get_ports {LEDS[2]}]
set_property PULLDOWN true [get_ports reset]
```

Software Design - Vitis

For SDK project creation, follow instructions from:

Vitis

Application

Template location: ./sw_lib/sw_apps/

hello_te0711

Hello TE0711 is a Xilinx Hello World example as endless loop instead of one console output.

Additional Software

No additional software is needed.

Appx. A: Change History and Legal Notices

Document Change History

To get content of older revision got to "Change History" of this page and select older document revision number.

Date	Document Revision	Authors	Description

2020-09-02	v.9	John Hartfiel	• 2019.2 release • Docu update
2018-11-30	v.8	John Hartfiel	• correction download link
2017-12-07	v.7	John Hartfiel	• 2017.2 release
	All	John Hartfiel	

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