

# TE0803 SK Demo1

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## Overview

Refer to <http://trenz.org/te0803-info> for the current online version of this manual and other available documentation.

## Key Features

- Vitis/Vivado 2019.2
- PetaLinux
- Linux Debian 9 (Stretch) or Linux Ubuntu 18.04 (Bionic Beaver)
- DisplayPort
- SD
- ETH (use EEPROM MAC)
- MAC from EEPROM
- PCIe
- USB
- I2C
- TEBF0808
- RGPIO
- SATA
- user LED access
- Modified FSBL for SI5338 programming
- Special FSBL for QSPI programming

## Revision History

Date	Vivado	Project Built	Authors	Description
2020-05-08	2019.2	TE0803-SK_DEMO1_noprebuilt-vivado_2019.2-build_11_20200508143345.zip TE0803-SK_DEMO1-vivado_2019.2-build_11_20200508143327.zip	Mohsen Chamanbaz	<ul style="list-style-type: none"><li>• initial release</li></ul>

### Design Revision History

## Release Notes and Know Issues

Issues	Description	Workaround	To be fixed version
No known issues	---	---	---

### Known Issues

## Requirements

### Software

Software	Version	Note
Vitis	2019.2	needed, Vivado is included into Vitis installation
PetaLinux	2019.2	needed
SD Card Formatter		format SD Card
Win32 DiskImager		burn generated image on SD
SI ClockBuilder Pro	----	optional

### Software

# Hardware

Basic description of TE Board Part Files is available on [TE Board Part Files](#).

Complete List is available on <design name>/board\_files/\*\_board\_files.csv

Design supports following modules:

Module Model	Board Part Short Name	PCB Revision Support	DDR	QSPI Flash	EMMC	Others	Notes
<del>TE0803-ES1</del>	es1_2gb	REV01	2GB	64MB	NA	NA	Not longer supported by vivado
TE0803-01-02EG-1E	2eg_2gb	REV01	2GB	64MB	NA	NA	NA
TE0803-01-02CG-1E	2cg_2gb	REV01	2GB	64MB	NA	NA	NA
TE0803-01-03EG-1E	3eg_2gb	REV01	2GB	64MB	NA	NA	NA
TE0803-01-03CG-1E	3cg_2gb	REV01	2GB	64MB	NA	NA	NA
TE0803-01-02EG-1EA	2eg_2gb	REV01	2GB	128MB	NA	NA	NA
TE0803-01-02CG-1EA	2cg_2gb	REV01	2GB	128MB	NA	NA	NA
TE0803-01-03EG-1EA	3eg_2gb	REV01	2GB	128MB	NA	NA	NA
TE0803-01-03CG-1EA	3cg_2gb	REV01	2GB	128MB	NA	NA	NA
TE0803-02-03EG-1EB	3eg_4gb	REV02 REV01	4GB	128MB	NA	NA	NA
TE0803-01-04CG-1EA	4cg_2gb	REV01	2GB	128MB	NA	NA	NA
TE0803-01-04EV-1EA	4ev_2gb	REV01	2GB	128MB	NA	NA	NA
TE0803-01-04EV-1E3	4ev_2gb	REV01	2GB	128MB	NA	1 mm connectors	NA
TE0803-01-04EG-1EA	4eg_2gb	REV01	2GB	128MB	NA	NA	NA
TE0803-01-04CG-1EB	4cg_2gb	REV01	2GB	256MB	NA	NA	NA
TE0803-01-05EV-1EA	5ev_2gb	REV01	2GB	128MB	NA	NA	NA
TE0803-01-05EV-1IA	5ev_i_2gb	REV01	2GB	128MB	NA	NA	NA
TE0803-02-04EV-1EB	4ev_4gb	REV02	4GB	128MB	NA	NA	NA
TE0803-02-04EV-1E3	4ev_4gb	REV02	4GB	128MB	NA	1 mm connectors	NA
TE0803-02-04EG-1E3	4eg_4gb	REV02	4GB	128MB	NA	1 mm connectors	NA
TE0803-03-2AE11-A	2cg_2gb	REV03	2GB	128MB	NA	NA	NA
TE0803-03-2BE11-A	2eg_2gb	REV03	2GB	128MB	NA	NA	NA
TE0803-03-3AE11-A	3cg_2gb	REV03	2GB	128MB	NA	NA	NA
TE0803-03-3BE11-A	3eg_2gb	REV03	2GB	128MB	NA	NA	NA
TE0803-03-4AE11-A	4cg_2gb	REV03	2GB	128MB	NA	NA	NA
TE0803-03-4BE11-A	4eg_2gb	REV03	2GB	128MB	NA	NA	NA
TE0803-03-4BE21-L	4eg_4gb	REV03	4GB	128MB	NA	1 mm connectors	NA
TE0803-03-4BI21-A	4eg_i_4gb	REV03	4GB	128MB	NA	NA	NA
TE0803-03-4DE11-A	4ev_2gb	REV03	2GB	128MB	NA	NA	NA
TE0803-03-4DE21-L	4ev_4gb	REV03	4GB	128MB	NA	1 mm connectors	NA
TE0803-03-4GE21-L	4eg_2_4gb	REV03	4GB	128MB	NA	1 mm connectors	NA
TE0803-03-5DE11-A	5ev_2gb	REV03	2GB	128MB	NA	NA	NA
TE0803-03-5DI21-A	5ev_i_4gb	REV03	4GB	128MB	NA	NA	NA
TE0803-03-3RI21-A	3eg_li_4gb	REV03	4GB	128MB	NA	NA	NA
TE0803-03-3BI21-A	3eg_i_4gb	REV03	4GB	128MB	NA	NA	NA
TE0803-03-4DI21-L	4ev_i_4gb	REV03	4GB	128MB	NA	1 mm connectors	NA
TE0803-03-4GI11-A	4eg_2i_2gb	REV03	2GB	128MB	NA	NA	NA
TE0803-03-4GE11-A	4eg_2_2gb	REV03	2GB	128MB	NA	NA	NA
TE0803-03-4GI21-A	4eg_2i_4gb	REV03	4GB	128MB	NA	NA	NA

TE0803-03-5BE11-A	5eg_2gb	REV03	2GB	128MB	NA	NA	NA
TE0803-03-5DI24-A	5ev_i_4gb	REV03	4GB	512MB	NA	NA	NA
TE0803-03-4BI21-X	4eg_i_4gb	REV03	4GB	128MB	NA	NA	U41 replaced with diode
TE0803-03-3BE21-A	3eg_4gb	REV03	4GB	128MB	NA	NA	NA
TE0803-03-3AE10-A	3cg_0_2gb	REV03	2GB	NA	NA	NA	NA
TE0803-03-3AE10-A	3cg_0_2gb	REV03	2GB	NA	NA	NA	NA

#### Hardware Modules

Design supports following carriers:

Carrier Model	Notes
TEBF0808	Used as reference carrier. <b>Important:</b> CPLD Firmware REV07 or newer is recommended

#### Hardware Carrier

Additional HW Requirements:

Additional Hardware	Notes
Cooler	It's recommended to use cooler on ZynqMP device
USB Cable	Connect to USB2 or better USB3 Hub for proper power supply over USB
DP Monitor	Optional HW Not all monitors are supported, also Adapter to other Standard can make drouble. Design was testet with <b>DELL U2412M</b>
Micro USB to USB A Adapter	Adapter for USB Hub
USB HUB	To connnect Mouse and Keyboard simultaneously
USB Keyboard	need for Ubuntu/Debian GUI
USB Mouse	need for Ubuntu/Debian GUI
DP Cable	--
Sata Disk	Optional HW
SATA Cable	Optional HW
PCIe Card	Optional HW
ETH Cable	Optional HW Ethernet works with DHCP, but can be setup also manually
SD Card	16GB

#### Additional Hardware

## Content

For general structure and of the reference design, see [Project Delivery - AMD devices](#)

## Design Sources

Type	Location	Notes
------	----------	-------

Vivado	<design name>/block_design <design name>/constraints <design name>/ip_lib	Vivado Project will be generated by TE Scripts
Vitis	<design name>/sw_lib	Additional Software Template for Vitis and apps_list.csv with settings automatically for Vitis app generation
PetaLinux	<design name>/os/petalinux	PetaLinux template with current configuration

#### Design sources

## Additional Sources

Type	Location	Notes
SI5338	<design name>/misc/SI5338	SI5338 Project with current PLL Configuration

#### Additional design sources

## Prebuilt

File	File-Extension	Description
BIF-File	*.bif	File with description to generate Bin-File
BIN-File	*.bin	Flash Configuration File with Boot-Image (Zynq-FPGAs)
BIT-File	*.bit	FPGA (PL Part) Configuration File
DebugProbes-File	*.ltx	Definition File for Vivado/Vivado Labtools Debugging Interface
Debian SD-Image	*.img	Debian Image for SD-Card
Diverse Reports	---	Report files in different formats
Hardware-Platform-Specification-Files	*.xsa	Exported Vivado Hardware Specification for Vitis and PetaLinux
LabTools Project-File	*.lpr	Vivado Labtools Project File
OS-Image	*.ub	Image with Linux Kernel (On Petalinux optional with Devicetree and RAM-Disk)
Image	---	Generic Linux kernel binary image file
Software-Application-File	*.elf	Software Application for Zynq or MicroBlaze Processor Systems
Device Tree Blob File	*.dtb	Contains a Device Tree Blob

#### Prebuilt files (only on ZIP with prebuilt content)

## Download

Reference Design is only usable with the specified Vivado/Vitis/PetaLinux version. Do never use different Versions of Xilinx Software for the same Project.

Reference Design is available on:

- [TE0803 "SK DEMO1" Reference Design](#)

## Design Flow



Reference Design is available with and without prebuilt files. It's recommended to use TE prebuilt files for first lunch.

Trenz Electronic provides a tcl based built environment based on Xilinx Design Flow.

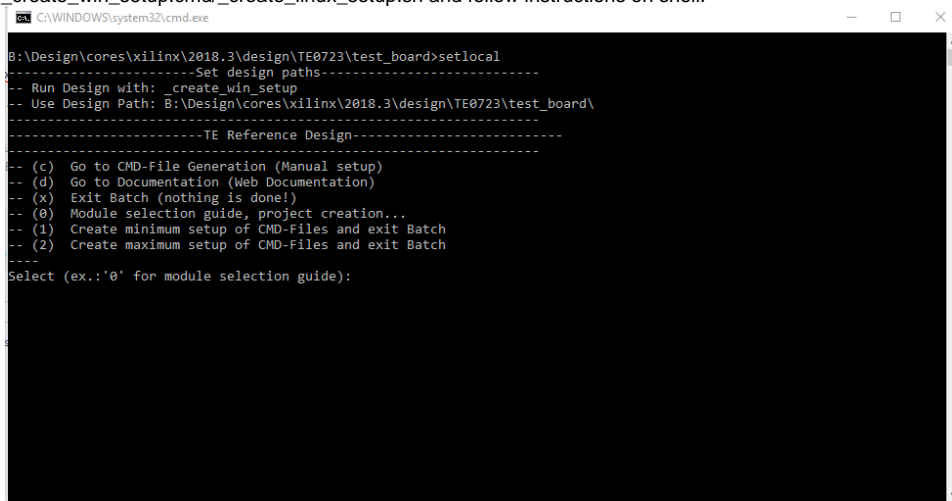
See also:

- [AMD Development Tools#XilinxSoftware-BasicUserGuides](#)
- [Vivado Projects - TE Reference Design](#)
- [Project Delivery.](#)

The Trenz Electronic FPGA Reference Designs are TCL-script based project. Command files for execution will be generated with "\_create\_win\_setup.cmd" on Windows OS and "\_create\_linux\_setup.sh" on Linux OS.

TE Scripts are only needed to generate the vivado project, all other additional steps are optional and can also be executed by Xilinx Vivado/SDK GUI. For currently Scripts limitations on Win and Linux OS see: [Project Delivery Currently limitations of functionality](#)

1. \_create\_win\_setup.cmd/\_create\_linux\_setup.sh and follow instructions on shell:



2. Press 0 and enter to start "Module Selection Guide"
3. (optional Win OS) Generate Virtual Drive or use short directory for the reference design (for example x:\<design name>)
4. Create Project (follow instruction of the product selection guide), settings file will be configured automatically during this process
  - a. (optional for manual changes) Select correct device and Xilinx install path on "design\_basic\_settings.cmd" and create Vivado project with "vivado\_create\_project\_guimode.cmd"  
Note: Select correct one, see also [TE Board Part Files](#)
    - i. **Important:** Use Board Part Files, which ends with \*\_tebf0808
5. Create XSA and export to prebuilt folder
  - a. Run on Vivado TCL: TE::hw\_build\_design -export\_prebuilt  
Note: Script generate design and export files into \prebuilt\hardware\<short dir>. Use GUI is the same, except file export to prebuilt folder
6. Create Linux (bl31.elf, uboot.elf, Image and system.dtb) with exported XSA
  - a. XSA is exported to "prebuilt\hardware\<short name>"  
Note: HW Export from Vivado GUI create another path as default workspace.  
Create Linux images on VM, see [PetaLinux KICKstart](#)
    - i. Use TE Template from /os/petalinux/
    - ii. Execute the script file for Debian/Ubuntu
7. Add Linux files (bl31.elf, uboot.elf, Image and system.dtb) to prebuilt folder
  - a. "prebuilt\os\petalinux\<ddr size>" or "prebuilt\os\petalinux\<short name>"
8. Generate Programming Files with Vitis
  - a. Run on Vivado TCL: TE::sw\_run\_vitis -all  
Note: Scripts generate applications and bootable files, which are defined in "sw\_lib\apps\_list.csv"
  - b. (alternative) Start SDK with Vivado GUI or start with TE Scripts on Vivado TCL: TE::sw\_run\_vitis  
Note: TCL scripts generate also platform project, this must be done manually in case GUI is used. See [Vitis](#)
9. Preparing SD card for SD Filesystem and hard disk for HD Filesystem See Programming section

## Launch

## Programming



Check Module and Carrier TRMs for proper HW configuration before you try any design.

Xilinx documentation for programming and debugging: [Vivado/SDK/SDSoC-Xilinx Software Programming and Debugging](#)

## Get prebuilt boot binaries

1. `_create_win_setup.cmd/_create_linux_setup.sh` and follow instructions on shell
2. Press 0 and enter to start "Module Selection Guide"
  - a. Select assembly version
  - b. Validate selection
  - c. Select Create and open delivery binary folder

Note: Folder (`<project folder>/_binaries_<Artikel Name>`) with subfolder (`boot_<app name>`) for different applications will be generated

## QSPI

Not used in this example.

## SD

1. Format the SD Card with SD Card Formatter or other tool
2. Write the Debian image or Ubuntu image file on SD Card with Win32DiskImager
3. It will automatically in BOOT directory two DTB file generated
  - a. `system_sd.dtb` : This file ist used , if the root file system is located on SD card.
  - b. `system_harddisk.dtb` : This file ist used , if the root file system is located on hard disk.
  - c. Note: To use one of the DTB files, this file must be renamed to `system.dtb`
4. Rename the `system_sd.dtb` file in BOOT directory to `system.dtb`
5. Copy Petalinux Image (not use `image.ub`), `system.dtb` and `Boot.bin` files on SD-Card.
  - use files from (`<project folder>/_binaries_<Articel Name>/boot_linux` from generated binary folder, see: [Get prebuilt boot binaries](#)
  - or use prebuilt file location, see `<design_name>/prebuilt/readme_file_location.txt`
6. Set Boot Mode to SD-Boot.
  - Depends on Carrier, see carrier TRM.
7. Insert SD-Card in SD-Slot.

## JTAG

Not used on this Example.

## Usage

1. Prepare HW like described on section [TE0803 StarterKit#Programming](#)
  2. Connect UART USB (JTAG XMOD)
  3. Select SD Card as Boot Mode (or QSPI - depending on step 1)

Note: See TRM of the Carrier, which is used.
  4. (Optional) Insert PCIe Card (detection depends on Linux driver. Only some basic drivers are installed)
  5. (Optional) Connect Sata Disc
  6. (Optional) Connect DisplayPort Monitor (List of usable Monitors: <https://www.xilinx.com/support/answers/68671.html>)
  7. (Optional) Connect Network Cable
  8. Power On PCB
- Note: 1. ZynqMP Boot ROM loads PMU Firmware and FSBL from SD into OCM, 2. FSBL loads ATF(bl31.elf) and U-boot from SD/QSPI into DDR, 3. U-boot load Linux from SD into DDR.

## Linux

1. Open Serial Console (e.g. putty)
  - a. Speed: 115200

- b. COM Port: Win OS, see device manager, Linux OS see `dmesg |grep tty` (UART is \*USB1)
- 2. Linux Console:
  - Note: Wait until Linux boot finished For Linux Login use:
    - a. User Name: root
    - b. Password: root
- 3. You can use Linux shell now.
- 4. Debian Desktop
  - a. Use connected mouse + keyboard for interaction with GUI
  - b. Start the GUI with the command : `startx`
  - c. Web Browser Dillo open console and type `dillo` or use browser
  - d. open console and start video or audio with "`mplayer <video or audio file>`"
- 5. Ubuntu Desktop
  - a. Use connected mouse + keyboard for interaction with GUI
  - b. Start the GUI with the command : `startx`
  - c. Web Browser Mozilla firefox can be used.
  - d. Audio or Video file can also be performed directly in GUI

### Hard Disk (optional)

To locate root file system on Hard disk:

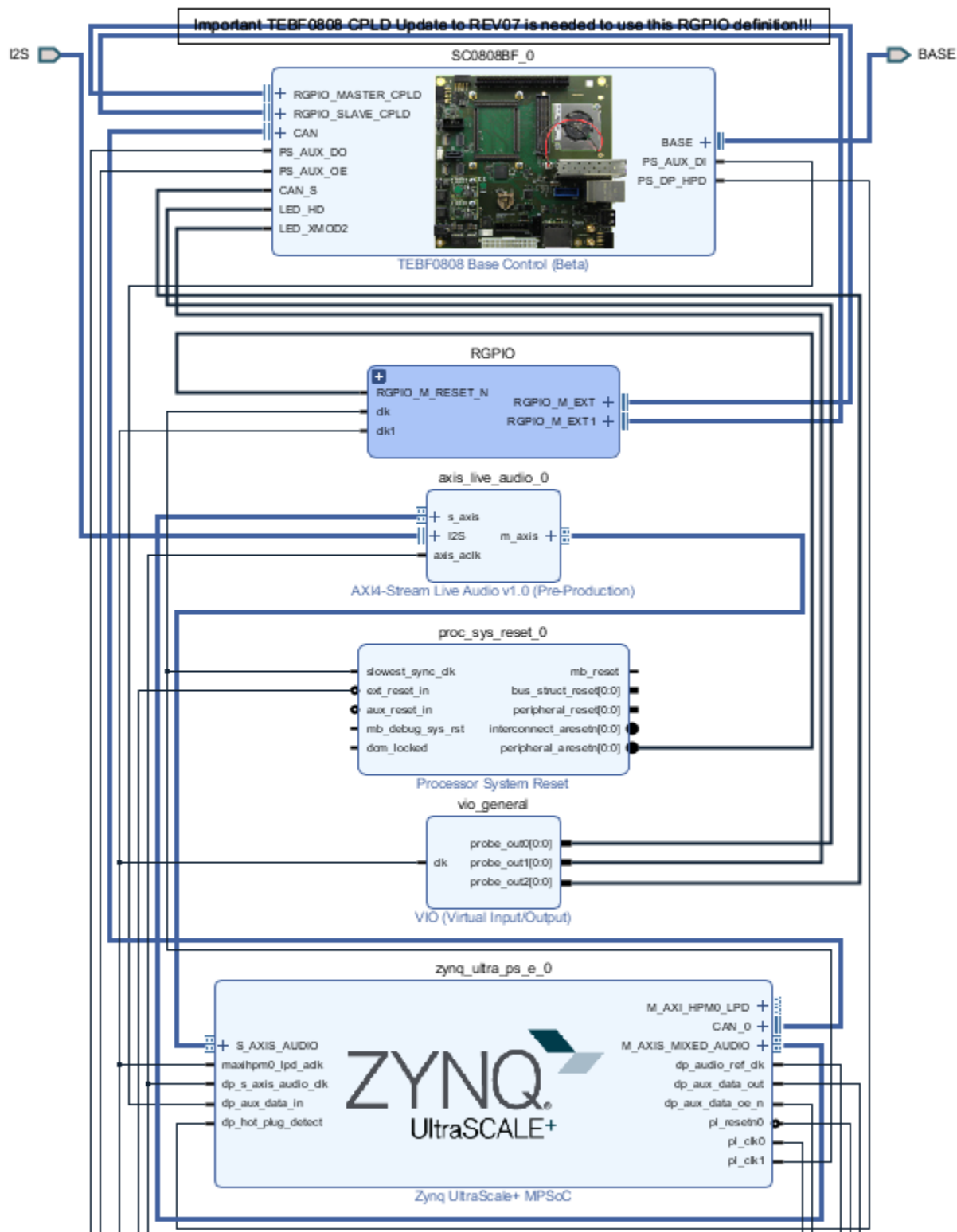
1. Plug in SD Card that you have prepared with root file system
2. Plug in Hard Disk in Sata port on the carrier board
3. Format the hard disk by the following command:
  - a. `mkfs.ext4 /dev/sda`
4. Edit the fstab file in directory `/etc/` to mount hard disk by the following commands:
  - a. `mkdir /media/harddisk`
  - b. `nano /etc/fstab`
  - c. Add this line to the fstab file and save it : `/dev/sda /media/harddisk/ defaults 0 3`
  - d. Reboot
5. Copy entire root file system in directory ROOTFS from SD card to hard disk by the following commands:
  - a. `cd /media/ROOTFS`
  - b. `cp -r / /media/harddisk`
6. Edit the fstab file in directory `/media/harddisk/etc/` by the following commands and save it:
  - a. `nano /media/harddisk/etc/fstab`
  - b. Edit this line to the fstab file : `/dev/sda /media/harddisk/ defaults 0 1`
  - c. Comment this line: `#/dev/mmcblk1p2 /media/ROOTFS defaults 0 1`
7. Shutdown the system
8. Format the SD card
9. Rename the Device Tree Blob file `system_harddisk.dtb` to `system.dtb`
10. Copy the following files to SD Card:
  - a. Image
  - b. BOOT.bin
  - c. system.dtb
11. Plug in the SD Card and turn on the system

## Vivado HW Manager

## System Design - Vivado

## Block Design







Block Design

PS Interfaces

Activated interfaces:

Type	Note
DDR	
QSPI	MIO
SD0	MIO
SD1	MIO
I2C0	MIO
UART0	MIO
GPIO0	MIO
SWDT0..1	
TTC0..3	
GEM3	MIO
USB0	MIO/GTP
SATA	GTP
DisplayPort	EMIO/GTP
PCIe	MIO/GTP
CAN0	EMIO
PJTAG0	MIO

PS Interfaces

Constrains

Basic module constrains

`_i_bitgen_common.xdc`

```
set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design]
set_property BITSTREAM.CONFIG.UNUSEDPIN PULLNONE [current_design]
```

Design specific constrain

## \_i\_io.xdc

```
# system controller ip
#LED_HD SC0 J3:31
#LED_XMOD SC17 J3:48
#CAN RX SC19 J3:52 B26_L11_P
#CAN TX SC18 J3:50 B26_L11_N
#CAN S SC16 J3:46 B26_L1_N

set_property PACKAGE_PIN G14 [get_ports BASE_sc0]
set_property PACKAGE_PIN D15 [get_ports BASE_sc5]
set_property PACKAGE_PIN H13 [get_ports BASE_sc6]
set_property PACKAGE_PIN H14 [get_ports BASE_sc7]
set_property PACKAGE_PIN A13 [get_ports BASE_sc10_io]
set_property PACKAGE_PIN B13 [get_ports BASE_sc11]
set_property PACKAGE_PIN A14 [get_ports BASE_sc12]
set_property PACKAGE_PIN B14 [get_ports BASE_sc13]
set_property PACKAGE_PIN F13 [get_ports BASE_sc14]
set_property PACKAGE_PIN G13 [get_ports BASE_sc15]
set_property PACKAGE_PIN A15 [get_ports BASE_sc16]
set_property PACKAGE_PIN B15 [get_ports BASE_sc17]
set_property PACKAGE_PIN J14 [get_ports BASE_sc18]
set_property PACKAGE_PIN K14 [get_ports BASE_sc19 ]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc0]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc5]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc6]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc7]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc10_io]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc11]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc12]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc13]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc14]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc15]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc16]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc17]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc18]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc19]

# Audio Codec
#LRCLK J3:49
#BCLK J3:51
#DAC_SDATA J3:53
#ADC_SDATA J3:55
set_property PACKAGE_PIN L13 [get_ports I2S_lrclk ]
set_property PACKAGE_PIN L14 [get_ports I2S_bclk ]
set_property PACKAGE_PIN E15 [get_ports I2S_sdin ]
set_property PACKAGE_PIN F15 [get_ports I2S_sdout ]
set_property IOSTANDARD LVCMOS18 [get_ports I2S_lrclk ]
set_property IOSTANDARD LVCMOS18 [get_ports I2S_bclk ]
set_property IOSTANDARD LVCMOS18 [get_ports I2S_sdin ]
set_property IOSTANDARD LVCMOS18 [get_ports I2S_sdout ]
```

For SDK project creation, follow instructions from:

[Vitis](#)

## Application

Template location: ./sw\_lib/sw\_apps/

### zynqmp\_fsbl

TE modified 2019.2 FSBL

General:

- Modified Files: xfsbl\_main.c, xfsbl\_hooks.h/.c, xfsbl\_board.h/.c(search for 'TE Mod' on source code)
- Add Files: te\_xfsbl\_hooks.h/.c (for hooks and board)\n\
- General Changes:
  - Display FSBL Banner and Device Name

Module Specific:

- Add Files: all TE Files start with te\_\*
  - Si5338 Configuration
  - OTG+PCIe Reset over MIO
  - I2C MUX for EEPROM MAC

### zynqmp\_fsbl\_flash

TE modified 2019.2 FSBL

General:

- Modified Files: xfsbl\_initialisation.c, xfsbl\_hw.h, xfsbl\_handoff.c, xfsbl\_main.c
- General Changes:
  - Display FSBL Banner
  - Set FSBL Boot Mode to JTAG
  - Disable Memory initialisation

### zynqmp\_pmufw

Xilinx default PMU firmware.

### hello\_te0803

Hello TE0803 is a Xilinx Hello World example as endless loop instead of one console output.

### u-boot

U-Boot.elf is generated with PetaLinux. Vitis is used to generate Boot.bin.

## Software Design - PetaLinux

For PetaLinux installation and project creation, follow instructions from:

- [PetaLinux KICKstart](#)

## Config

Start with **petalinux-config** or **petalinux-config --get-hw-description**

Select Image Packaging Configuration ==> Root filesystem type ==> Select SD Card

Changes:

- CONFIG\_SUBSYSTEM\_PRIMARY\_SD\_PSU\_SD\_1\_SELECT=y
- CONFIG\_SUBSYSTEM\_ETHERNET\_PSU\_ETHERNET\_3\_MAC=""
- # CONFIG\_SUBSYSTEM\_BOOTARGS\_AUTO is not set
- CONFIG\_SUBSYSTEM\_USER\_CMDLINE="console=ttyPS0,115200 earlycon clk\_ignore\_unused earlyprintk root=/dev/mmcblk1p2 rootfstype=ext4 rw rootwait cma=1024M"
- CONFIG\_SUBSYSTEM\_DEVICETREE\_FLAGS=""
- # CONFIG\_SUBSYSTEM\_IMAGES\_ADVANCED\_AUTOCONFIG\_DTB\_MEDIA\_BOOTIMAGE\_SELECT is not set
- # CONFIG\_SUBSYSTEM\_IMAGES\_ADVANCED\_AUTOCONFIG\_DTB\_MEDIA\_FLASH\_SELECT is not set
- CONFIG\_SUBSYSTEM\_IMAGES\_ADVANCED\_AUTOCONFIG\_DTB\_MEDIA\_SD\_SELECT=y
- # CONFIG\_SUBSYSTEM\_IMAGES\_ADVANCED\_AUTOCONFIG\_DTB\_MEDIA\_ETHERNET\_SELECT is not set
- # CONFIG\_SUBSYSTEM\_IMAGES\_ADVANCED\_AUTOCONFIG\_DTB\_MEDIA\_MANUAL\_SELECT is not set
- CONFIG\_SUBSYSTEM\_IMAGES\_ADVANCED\_AUTOCONFIG\_DTB\_IMAGE\_NAME="system.dtb"
- CONFIG\_SUBSYSTEM\_ENDIAN\_LITTLE=y
- # CONFIG\_SUBSYSTEM\_IMAGES\_ADVANCED\_AUTOCONFIG\_KERNEL\_MEDIA\_FLASH\_SELECT is not set
- CONFIG\_SUBSYSTEM\_IMAGES\_ADVANCED\_AUTOCONFIG\_KERNEL\_MEDIA\_SD\_SELECT=y
- # CONFIG\_SUBSYSTEM\_IMAGES\_ADVANCED\_AUTOCONFIG\_KERNEL\_MEDIA\_ETHERNET\_SELECT is not set
- # CONFIG\_SUBSYSTEM\_IMAGES\_ADVANCED\_AUTOCONFIG\_KERNEL\_MEDIA\_MANUAL\_SELECT is not set
- CONFIG\_SUBSYSTEM\_IMAGES\_ADVANCED\_AUTOCONFIG\_KERNEL\_IMAGE\_NAME="Image"

## U-Boot

Start with **petalinux-config -c u-boot**

Changes:

- CONFIG\_ENV\_IS\_NOWHERE=y
- # CONFIG\_ENV\_IS\_IN\_SPI\_FLASH is not set
- CONFIG\_I2C\_EEPROM=y
- CONFIG\_ZYNQ\_GEM\_I2C\_MAC\_OFFSET=0xFA
- CONFIG\_SYS\_I2C\_EEPROM\_ADDR=0x50
- CONFIG\_SYS\_I2C\_EEPROM\_BUS=2
- CONFIG\_SYS\_EEPROM\_SIZE=256
- CONFIG\_SYS\_EEPROM\_PAGE\_WRITE\_BITS=0
- CONFIG\_SYS\_EEPROM\_PAGE\_WRITE\_DELAY\_MS=0
- CONFIG\_SYS\_I2C\_EEPROM\_ADDR\_LEN=1
- CONFIG\_SYS\_I2C\_EEPROM\_ADDR\_OVERFLOW=0

## Device Tree

```
/include/ "system-conf.dtsi"
/ {
    chosen {
        xlnx,eeeprom = &eeeprom;
        bootargs= "console=ttyPS0,115200 earlycon clk_ignore_unused earlyprintk root=/dev/mmcblk1p2
rootfstype=ext4 rw rootwait cma=1024M";
        /* notes: root=/dev/mmcblk1p2 for SD and root=/dev/sda for hard disk will be changed
automatically by executing debian/ubuntu script*/
    };
};

/* notes:
serdes: // PHY TYP see: dt-bindings/phy/phy.h
*/
```

```

/* default */

/* SD */

&sdhci1 {
    disable-wp;
    no-1-8-v;
};

/* USB */

&dwc3_0 {
    status = "okay";
    dr_mode = "host";
    snps,usb3_lpm_capable;
    snps,dis_u3_susphy_quirk;
    snps,dis_u2_susphy_quirk;
    phy-names = "usb2-phy", "usb3-phy";
    phys = <&lane1 4 0 2 100000000>;
    maximum-speed = "super-speed";
};

/* ETH PHY */

&gem3 {
    phy-handle = <&phy0>;
    phy0: phy0@1 {
        device_type = "ethernet-phy";
        reg = <1>;
    };
};

/* QSPI */

&qspi {
    #address-cells = <1>;
    #size-cells = <0>;
    status = "okay";
    flash0: flash@0 {
        compatible = "jedec,spi-nor";
        reg = <0x0>;
        #address-cells = <1>;
        #size-cells = <1>;
    };
};

/* I2C */

&i2c0 {
    i2cswitch@73 { // u
        compatible = "nxp,pca9548";
        #address-cells = <1>;
        #size-cells = <0>;
        reg = <0x73>;
        i2c-mux-idle-disconnect;
        i2c@0 { // MCLK TEBF0808 SI5338A, 570FBB000290DG_unassembled

```

```

        #address-cells = <1>;
        #size-cells = <0>;
        reg = <0>;
    };
    i2c@1 { // SFP TEBF0808 PCF8574DWR
        #address-cells = <1>;
        #size-cells = <0>;
        reg = <1>;
    };
    i2c@2 { // PCIe
        #address-cells = <1>;
        #size-cells = <0>;
        reg = <2>;
    };
    i2c@3 { // SFP1 TEBF0808
        #address-cells = <1>;
        #size-cells = <0>;
        reg = <3>;
    };
    i2c@4 { // SFP2 TEBF0808
        #address-cells = <1>;
        #size-cells = <0>;
        reg = <4>;
    };
    i2c@5 { // TEBF0808 EEPROM
        #address-cells = <1>;
        #size-cells = <0>;
        reg = <5>;
        eeprom: eeprom@50 {
            compatible = "atmel,24c08";
            reg = <0x50>;
        };
    };
    i2c@6 { // TEBF0808 FMC
        #address-cells = <1>;
        #size-cells = <0>;
        reg = <6>;
    };
    i2c@7 { // TEBF0808 USB HUB
        #address-cells = <1>;
        #size-cells = <0>;
        reg = <7>;
    };
};
i2cswitch@77 { // u
    compatible = "nxp,pca9548";
    #address-cells = <1>;
    #size-cells = <0>;
    reg = <0x77>;
    i2c-mux-idle-disconnect;
    i2c@0 { // TEBF0808 PMOD P1
        #address-cells = <1>;
        #size-cells = <0>;
        reg = <0>;
    };
    i2c@1 { // i2c Audio Codec
        #address-cells = <1>;
        #size-cells = <0>;
        reg = <1>;
        /*
        adaul761: adaul761@38 {

```





Applications will be generated with Debian script or Ubuntu script (mkdebian\_stretch.sh/mkubuntu\_BionicBeaver.sh)

## Additional Software

No additional software is needed.

## SI5338

File location <design name>/misc/SI5338/SI5338-\*.slabtimeproj

General documentation how you work with these project will be available on [SI5338](#)

## Appx. A: Change History and Legal Notices

### Document Change History

To get content of older revision got to "Change History" of this page and select older document revision number.

Date	Document Revision	Authors	Description
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<div data-bbox="235 394 487 457"><b>Error rendering macro 'page-info'</b></div> <div data-bbox="235 495 487 1234"><p>Ambiguous method overloading for method jdk.proxy241.\$Proxy3496#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]</p></div>	<div data-bbox="644 394 896 457"><b>Error rendering macro 'page-info'</b></div> <div data-bbox="644 495 896 1234"><p>Ambiguous method overloading for method jdk.proxy241.\$Proxy3496#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]</p></div>	<div data-bbox="1050 394 1302 457"><b>Error rendering macro 'page-info'</b></div> <div data-bbox="1050 495 1302 1234"><p>Ambiguous method overloading for method jdk.proxy241.\$Proxy3496#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]</p></div>	<div data-bbox="1386 323 1468 365"><ul style="list-style-type: none"><li>• 2019.2 release</li></ul></div>
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--	all	<div> <p><b>Error rendering macro 'page-info'</b></p> <p>Ambiguous method overloading for method jdk.proxy241.\$Proxy3496#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]</p> </div>	--
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Document change history.

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Please also note our data protection declaration at <https://www.trenz-electronic.de/en/Data-protection-Privacy>

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Ambiguous method overloading for method `jdk.proxy241.$Proxy3496#hasContentLevelPermission`. Cannot resolve which method to invoke for `[null, class java.lang.String, class com.atlassian.confluence.pages.Page]` due to overlapping prototypes between: `[interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]` `[interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]`