TE0823 TRM

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Overview

The Trenz Electronic TE0823 (3PIU1FA /3PIU1FL) is an industrial-grade MPSoC module integrating a low power Xilinx Zynq UltraScale+ MPSoC, 1 GByte LPDDR4 SDRAM, 8 GB eMMC chip, 2x 64 MB Flash memory for configuration and operation, and powerful switch-mode power supplies for all on-board voltages. A large number of configurable I/O's is provided via rugged high-speed stacking connections. The module is equipped with a Lattice Mach XO2 CPLD for system controlling. 3x Robust high-speed connectors provide a large number of inputs and outputs.

The highly integrated modules are smaller than a credit card and are offered in several variants at an affordable price-performance ratio. Modules with a 4 x 5 cm form factor are completely mechanically and largely electrically compatible with each other.

All parts are at least industrial temperature range. The module operating temperature range depends on customer design and cooling solution. Please contact us for options.

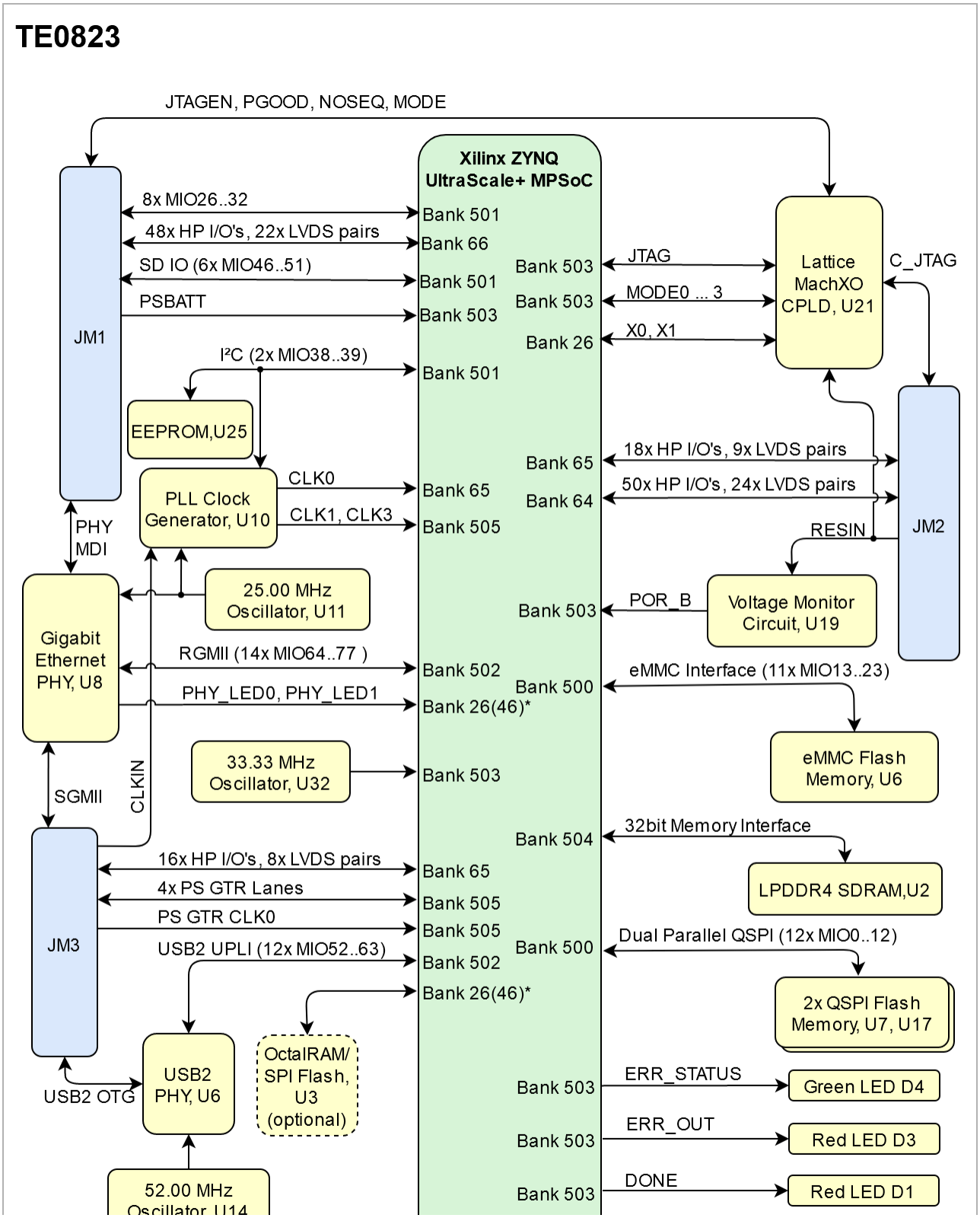
Refer to http://trenz.org/te0823-info for the current online version of this manual and other available documentation.

Key Features

- **SoC/FPGA**
  - Package: SFVC784, SFRC784
  - Device: ZU2 ...ZU5, *
  - Engine: EG, CG, EV, *
  - Speed: -1, -1L, -2, -2L, 3, *, **
  - Temperature: I, E, *, **
- **RAM/Storage**
  - 2x DDR4 SDRAM,
    - Data Width: 32 Bit
    - Size: 16 Gb, *
    - Speed: 3733 Mbps, ***
  - 2x QSPI boot Flash in dual parallel mode
    - Data Width: 8 Bit
    - Size: 512 Mb Gb, *
  - 1x e.MMC Memory
    - Data Width: 8 Bit
    - Size: 32 Gb, *
  - MAC address serial EEPROM
- **On Board**
  - Lattice MachXO2 CPLD
  - Programmable Clock Generator
  - Hi-speed USB2 ULPI Transceiver
  - 4x LEDS
- **Interface**
  - 1x GB/s serial GMII interface
  - 1x Hi-speed USB2 ULPI transceiver with full OTG support
  - 154 x High Performance (HP) und 96 x High Density (HD) I/Os
  - 78 x PS MIOs
  - 4 x serial PS GTR transceivers
    - PCI Express interface version 2.1 compliant
    - SATA 3.1 specification compliant interface
    - DisplayPort source-only interface with video resolution up to 4k x 2k
    - USB 3.0 specification compliant interface implementing a 5 Gbit/s line rate
- **Power**
  - All power regulators on board
- **Dimension**
  - 40 x 50 mm
- **Note**
  - * depends on assembly version
  - ** also non low power assembly options possible
  - *** depends on used U+ Zynq and DDR4 combination
  - Rugged for shock and high vibration

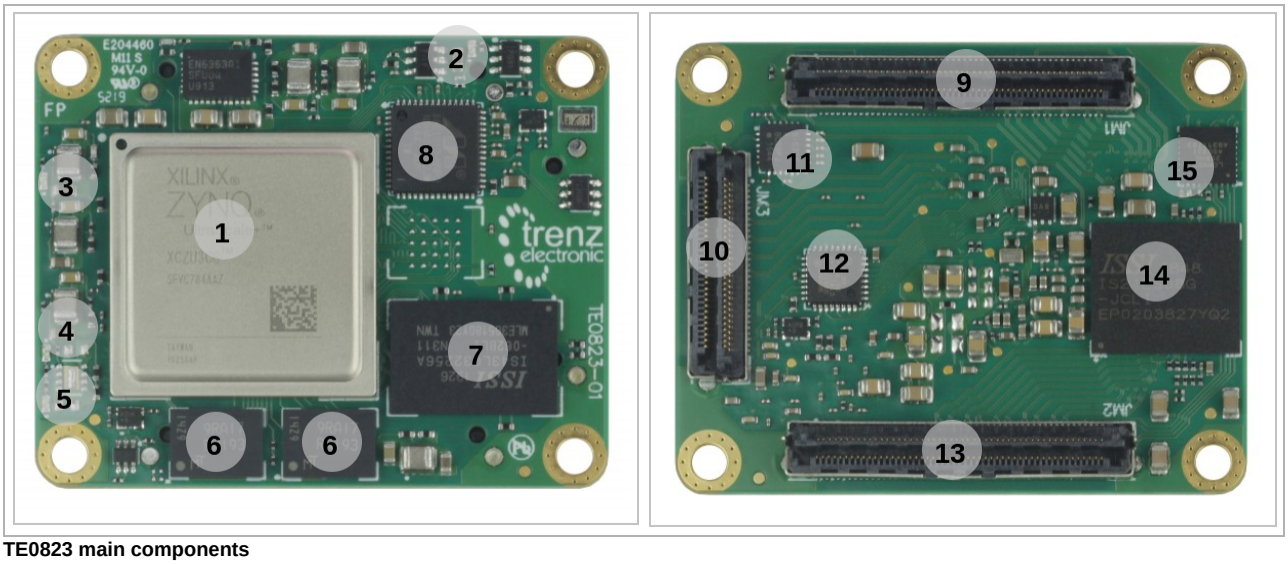
Block Diagram

TE0823


JTAGEN, PGOOD, NOSEQ, MODE
Xilinx ZYNQ UltraScale+ MPSoC
JM1
8x MIO26..32
Bank 501
48x HP I/O's, 22x LVDS pairs
Bank 66
SD IO (6x MIO46..51)
Bank 501
PSBATT
Bank 503
I²C (2x MIO38..39)
Bank 501
EEPROM,U25
PLL Clock Generator, U10
CLK0
CLK1, CLK3
Bank 65
Bank 505
PHY MDI
25.00 MHz Oscillator, U11
Gigabit Ethernet PHY, U8
RGMII (14x MIO64..77)
PHY_LED0, PHY_LED1
Bank 502
Bank 26(46)*
33.33 MHz Oscillator, U32
Bank 503
SGMII
CLKIN
JM3
16x HP I/O's, 8x LVDS pairs
4x PS GTR Lanes
PS GTR CLK0
USB2 UPLI (12x MIO52..63)
Bank 65
Bank 505
Bank 505
Bank 502
Bank 26(46)*
USB2 OTG
USB2 PHY, U6
OctalRAM/ SPI Flash, U3 (optional)
52.00 MHz Oscillator, U14
Bank 503
JTAG
MODE0 ... 3
X0, X1
Bank 503
Bank 503
Bank 26
Lattice MachXO CPLD, U21
C_JTAG
18x HP I/O's, 9x LVDS pairs
50x HP I/O's, 24x LVDS pairs
Bank 65
Bank 64
JM2
RESIN
POR_B
Voltage Monitor Circuit, U19
Bank 503
eMMC Interface (11x MIO13..23)
Bank 500
eMMC Flash Memory, U6
32bit Memory Interface
Bank 504
LPDDR4 SDRAM,U2
Dual Parallel QSPI (12x MIO0..12)
Bank 500
2x QSPI Flash Memory, U7, U17
ERR_STATUS
Bank 503
Green LED D4
ERR_OUT
Bank 503
Red LED D3
DONE
Bank 503
Red LED D1

TE0823 block diagram

Main Components



TE0823 main components

1. Xilinx Zynq UltraScale+ XCZU3EG, U1
2. Red LED (ERR_OUT), D3
3. Green User LED, D2
4. Green LED (ERR_STATUS), D4
5. Red LED (DONE), D1
6. 10/100/1000 Mbps energy efficient ethernet transceiver, U8
7. 8Gb DDR4, U2-U3
8. 512 Mbit QSPI flash memory, U7-U17
9. B2B connector Samtec Razor Beam, JM1
10. B2B connector Samtec Razor Beam, JM3
11. Programmable clock generator, U10
12. USB2.0 Transceiver, U18
13. B2B connector Samtec Razor Beam, JM2
14. 8 GByte eMMC memory, U6
15. Lattice Semiconductor MachXO2 System Controller CPLD, U21

Initial Delivery State

Storage device name	Content	Notes
QSPI Flash Memory	Not programmed	
eMMC Memory	Not programmed	
Programmable Clock Generator	Not programmed	
CPLD (LCMXO2-256HC)	SC0820-02 QSPI Firmware	

Initial delivery state of programmable devices on the module

Configuration Signals

MODE Signal State	Boot Mode
High	QSPI*
Low	SD Card*

*changable also with other CPLD Firmware:TE0823 CPLD
Boot process.

Signal	B2B	I/O	Note
RESIN	JM2-18	Input	

Reset process.

Signals, Interfaces and Pins

Board to Board (B2B) I/Os

FPGA bank number and number of I/O signals connected to the B2B connector:

FPGA Bank	B2B Connector	I/O Signal Count	Voltage Level	Notes	
24	HD	JM2	24x I/O, 12x LVDS Pairs	Variable	Max voltage 3.3V
25	HD	JM1	24x I/O, 12x LVDS Pairs	Variable	Max voltage 3.3V
26	HD	JM1	24x I/O, 12x LVDS Pairs	Variable	Max voltage 3.3V
44	HD	JM2	24x I/O, 12x LVDS Pairs	Variable	Max voltage 3.3V
65	HP	JM2	18x I/O, 9x LVDS Pairs	Variable	Max voltage 1.8V
65	HP	JM3	16x I/O, 8x LVDS Pairs	Variable	Max voltage 1.8V
505	GTR	JM3	16x I/O, 8x LVDS Pairs	-	4x lanes
505	GTR CLK	JM3	1x Diff Clock	-	
501	MIO	JM1	15 I/O	3.3V	

General PL I/O to B2B connectors information

JTAG Interface

JTAG access to the Xilinx Zynq UltraScale+ is applicable by using Lattice MachXO CPLD through B2B connector JM2.

JTAG Signal	B2B Connector	Notes
TMS	JM2-93	
TDI	JM2-95	
TDO	JM2-97	
TCK	JM2-99	

JTAGEN	JM1-89	Pulled Low: Xilinx Zynq UltraScale+ MPSoC Pulled High: Lattice MachXO CPLD

JTAG pins connection

MGT Lanes

There are 4x MGT Lanes connected to FPGA Bank 505-GTR.

Lane	Schematic	B2B	Note
0	• B505_RX0_P • B505_RX0_N • B505_TX0_P • B505_TX0_N	• JM3-26 • JM3-28 • JM3-25 • JM3-27	
1	• B505_RX1_P • B505_RX1_N • B505_TX1_P • B505_TX1_N	• JM3-20 • JM3-22 • JM3-19 • JM3-21	
2	• B505_RX2_P • B505_RX2_N • B505_TX2_P • B505_TX2_N	• JM3-14 • JM3-16 • JM3-13 • JM3-15	
3	• B505_RX2_P • B505_RX2_N • B505_TX2_P • B505_TX2_N	• JM3-8 • JM3-10 • JM3-7 • JM3-9	

MGT Lanes connection

Gigabit Ethernet

On-board Gigabit Ethernet PHY is provided with Marvell Alaska 88E1512 chip. The Ethernet PHY RGMII interface is connected to the Zynq Ethernet0 PS GEM0. I/O voltage is fixed at 1.8V for HSTL signaling. SGMII (SFP copper or fiber) can be used directly with the Ethernet PHY, as the SGMII pins are available on the B2B connector JM3. The reference clock input of the PHY is supplied from an on-board 25MHz oscillator (U11), the 125MHz output clock is left unconnected.

Pin	Schematic	Connected to	Note
MDIP0...3	PHY_MDI0...3	B2B, JM1	
MDC	ETH_MDC	MIO76	
MDIO	ETH_MDIO	MIO77	
S_IN	S_IN	B2B, JM3	
S_OUT	S_OUT	B2B, JM3	
TXD0..3	ETH_TXD0...3	MIO65...68	
TX_CTRL	ETH_TXCTL	MIO69	
TX_CLK	ETH_TXCK	MIO64	
RXD0...3	ETH_RXD0...3	MIO71...74	
RX_CTRL	ETH_RXCTL	MIO75	

RX_CLK	ETH_RXCK	MIO70	
LED0...2	PHY_LED0...2	FPGA Bank 66	
RESETn	ETH_RST	MIO24	

GigaBit Ethernet connection

System Controller CPLD

Special purpose pins are connected to System Controller CPLD and have following default configuration:

Pin Name	Mode	Function	Default Configuration
EN1	Input	Power Enable	No hard wired function on PCB. When forced low, PGOOD goes low without effect on power management
PGOOD	Output	Power Good	Only indirect used for power status, see CPLD description
NOSEQ	-	-	No used for Power sequencing, see CPLD description
RESIN	Input	Reset	Active low reset, gated to POR_B
JTAGEN	Input	JTAG Select	Low for normal operation, high for CPLD JTAG access

System Controller CPLD special purpose pins

USB Interface

USB PHY is provided by Microchip USB3320. The ULPI interface is connected to the Zynq PS USB0. I/O voltage is fixed at 1.8V. Reference clock input for the USB PHY is supplied by the on-board 52.00 MHz oscillator (U14).

PHY Pin	ZYNQ Pin	B2B Name	Notes
ULPI	MIO52..63	-	Zynq USB0 MIO pins are connected to the USB PHY.
REFCLK	-	-	52.000000 MHz from on-board oscillator (U14).
REFSEL[0..2]	-	-	Reference clock frequency select, all set to GND selects 52.000000 MHz.
RESETB	MIO25	-	Active low reset.
CLKOUT	MIO52	-	Connected to 1.8V, selects reference clock operation mode.
DP, DM	-	OTG_D_P, OTG_D_N	USB data lines routed to B2B connector JM3 pins 47 and 49.
CPEN	-	VBUS_V_EN	External USB power switch active high enable signal, routed to JM3 pin 17.
VBUS	-	USB_VBUS	Connect to USB VBUS via a series of resistors, see reference schematics, routed to JM3 pin 55.
ID	-	OTG_ID	For an A-device connect to ground, for a B-device left floating. routed from JM3 pin 23.

General overview of the USB PHY signals

I2C Interface

On-board I^2C devices are connected to MIO38 (SCL) and MIO39 (SDA) which are configured as I^2C0 by default. Addresses for on-board I^2C slave devices are listed in the table below:

I2C Device	I2C Address	Notes
Si5338A PLL	0x70	-
EEPROM	0x50	-

Address table of the I2C bus slave devices

MIO Pins

MIO Pin	Connected to	B2B	Notes
0...5	QSPI Flash, U7	-	SPI Flash
7...12	QSPI Flash, U17	-	SPI Flash
13...23	eMMC, U6		
24	ETH Transceiver, U8	-	ETH_RST
25	USB2.0 Transceiver, U18	-	OTG_RST
26...33	User MIO	JM1	
34...37	N.C	-	N.C
38...39	EEPROM, U25	-	I2C_SDA/SCL
40...45	N.C		N.C
46...51	SD Card	JM1	
52...63	USB2.0 Transceiver, U18	-	
63...77	Ethernet Transceiver, U8	-	

MIOs pins

Test Points

Test Point	Signal	Connected to	Notes
1	PS_LP0V85	Regulator, U12	
2	SRST_B	FPGA Bank 503, U1H	PSCONFIG
3	PS_AVCC	Regulator, U9	
4	+1.1V_LPDDR4	Regulator, U15	
5	PS_AVTT	Regulator, U13	
6	-	-	
7	PS_FP0V85	Regulator, U26	
8	PS_LP0V85	Voltage Regulator, U12	
9	POR_B	Voltage Regulator, U19	
10	PS_PLL	Voltage Regulator, U23	
11	PL_VCCINT	Voltage Regulator, U5	
12...15	-	-	
16	PL_VCU	Voltage Regulator, U24	

Test Points Information

On-board Peripherals

Chip/Interface	Designator	Notes

QSPI Flash	U7, U17	
EEPROM	U25	
DDR4 SDRAM	U2,U3	
GigaBit Ethernet	U8	
USB2.0 Transceiver	U18	
eMMC Memory	U6	
Oscillators	U32, U14, U11	
Programmable Clock Generator	U25	
CPLD	U21	
LEDs	D1...3	

On board peripherals

Quad SPI Flash Memory

The TE0821 is equipped with dual Flash Memory, U7, U17. Two quad SPI compatible serial bus flash memory chips are provided for FPGA configuration file and data storage. After configuration completes the remaining free memory can be used for application data storage. All four SPI data lines are connected to the FPGA allowing x1, x2 or x4 data bus widths to be used. The maximum data transfer rate depends on the bus width and clock frequency.

Pin	Schematic		Notes
	QSPI, U7	QSPI, U17	
nCS	MIO5	MIO7	
CLK	MIO0	MIO12	
DI/IO0	MIO4	MIO8	
DO/IO1	MIO1	MIO9	
nHOLD/IO3	MIO3	MIO11	
WP/IO2	MIO2	MIO10	

Quad SPI interface MIOs and pins

EEPROM

There is a 2Kb EEPROM provided on the module TE0821.

MIO Pin	Schematic	U?? Pin	Notes
MIO39	I2C_SDA	SDA	
MIO38	I2C_SCL	SCL	

I2C EEPROM interface MIOs and pins

MIO Pin	I2C Address	Designator	Notes
MIO38-MIO39	0x50	U25	

I2C address for EEPROM

LEDs

Designator	Color	Connected to	Active Level	Note
D1	Red	DONE	Low	
D2	Green	USR_LED	High	
D3	Red	ERR_OUT	High	
D4	Green	ERR_STATUS	High	

On-board LEDs

DDR4 SDRAM

The TE0823 SoM has a 1 GB volatile LPDDR4 SDRAM IC for storing user application code and data.

- Part number: IS43LQ32256A
- Supply voltage: 1.7V ~ 1.95V
- Speed: 3200 Mbps
- Temperature: -40 ~ 95 °C

Gigabyte Ethernet

On-board Gigabit Ethernet PHY (U8) is provided with Marvell Alaska 88E1512 IC (U8). The Ethernet PHY RGMII interface is connected to the ZynqMP Ethernet3 PS GEM3. I/O voltage is fixed at 1.8V for HSTL signaling. The reference clock input of the PHY is supplied from an on-board 25.00 MHz oscillator (U11).

U8 Pin	Schematic	Connected to	Note
MDIP0...3	PHY_MDI0...3	B2B, JM1	
MDC	ETH_MDC	MIO76	
MDIO	ETH_MDIO	MIO77	
S_IN	S_IN	B2B, JM3	
S_OUT	S_OUT	B2B, JM3	
TXD0..3	ETH_TXD0...3	MIO65...68	
TX_CTRL	ETH_TXCTL	MIO69	
TX_CLK	ETH_TXCK	MIO64	
RXD0...3	ETH_RXD0...3	MIO71...74	
RX_CTRL	ETH_RXCTL	MIO75	
RX_CLK	ETH_RXCK	MIO70	
LED0...2	PHY_LED0...2	FPGA Bank 66	
RESETn	ETH_RST	MIO24	

Ethernet PHY to Zynq SoC connections

Clock Sources

Designator	Description	Frequency	Note

U11	MEMS Oscillator	25 MHz	
U14	MEMS Oscillator	52 MHz	
U32	MEMS Oscillator	80 MHz	

Osillators

USB2.0 Transceiver

Hi-speed USB ULPI PHY (U18) is provided with USB3320 from Microchip. The ULPI interface is connected to the Zynq PS USB0 via MIO52..63, bank 502. The I/O voltage is fixed at 1.8V and PHY reference clock input is supplied from the on-board 52.00 MHz oscillator (U14).

eMMC Flash Memory

eMMC Flash memory device(U6) is connected to the ZynqMP PS MIO bank 500 pins MIO13..MIO23. eMMC chips IS21ES08G-JCLI (FLASH - NAND Speicher-IC (64 Gb x 1) MMC) is used.

Programmable Clock Generator

There is a Silicon Labs I^2C programmable clock generator Si5338A (U10) chip on the module. It's output frequencies can be programmed using the I^2C bus address 0x70 or 0x71. Default address is 0x70, IN4/I2C_LSB pin must be set to high for address 0x71.

A 25.00 MHz oscillator is connected to the pin IN3 and is used to generate the output clocks. The oscillator has its output enable pin permanently connected to 1.8V power rail, thus making output frequency available as soon as 1.8V is present. Three of the Si5338 clock outputs are connected to the FPGA. One is connected to a logic bank and the other two are connected to the GTR banks.

Once running, the frequency and other parameters can be changed by programming the device using the I^2C bus connected between the FPGA (master) and clock generator (slave). For this, proper I^2C bus logic has to be implemented in FPGA.

U25 Pin	Signal	Connected to	Direction	Note
IN0..1	CLK_IN	JM3	IN	
IN2	CLK_25M	Oscillator, U11	IN	
SCL	I2C_SCL	EEPROM,U25	INOUT	
SDA	I2C_SDA	EEPROM,U25	INOUT	
CLK0	CLK0	JM3	OUT	
CLK1	B505_CLK3	FPGA Bank 505	IN	
CLK2	B505_CLK1	FPGA Bank 505	IN	
CLK3	CLK3_N		IN	

Programmable Clock Generator Inputs and Outputs

Power and Power-On Sequence

Power Supply

Power supply with minimum current capability of 2.5 A for system startup is recommended.

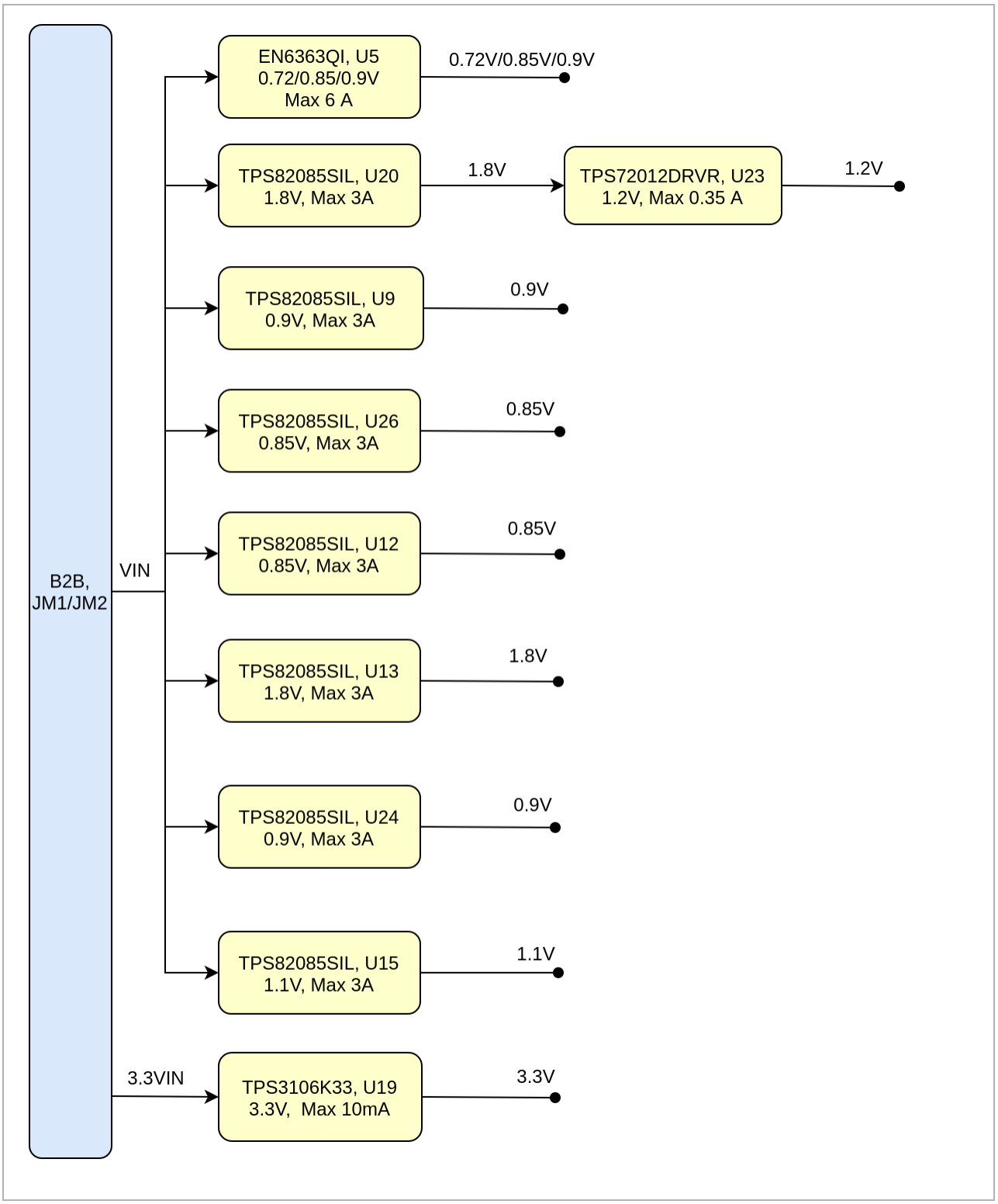
Power Consumption

Power Input Pin	Typical Current
VIN	TBD*

Power Consumption

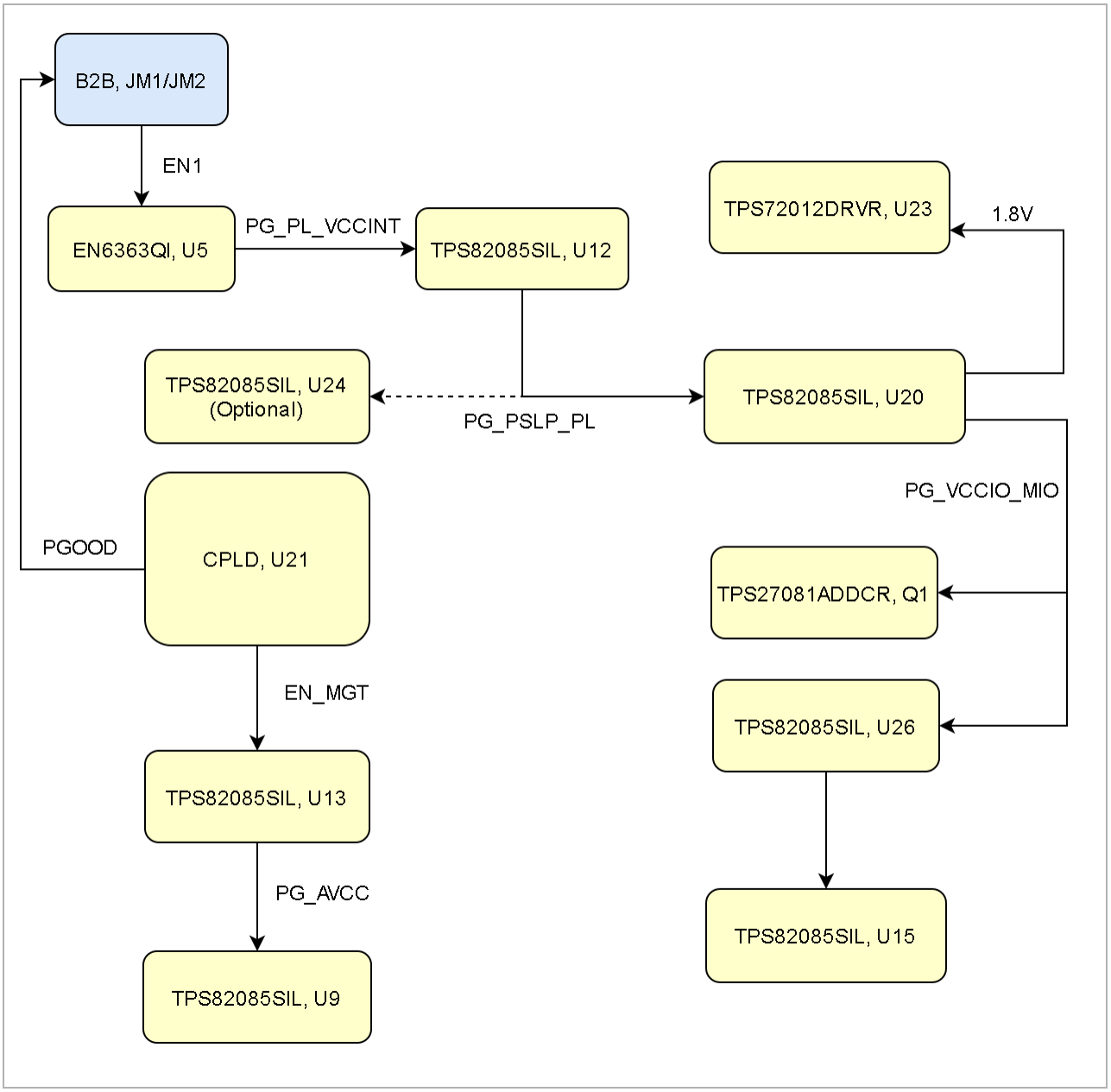
* TBD - To Be Determined

Power Distribution Dependencies


B2B,
JM1/JM2
VIN
3.3VIN
EN6363QI, U5
0.72/0.85/0.9V
Max 6 A
0.72V/0.85V/0.9V
TPS82085SIL, U20
1.8V, Max 3A
1.8V
TPS72012DRVR, U23
1.2V, Max 0.35 A
1.2V
TPS82085SIL, U9
0.9V, Max 3A
0.9V
TPS82085SIL, U26
0.85V, Max 3A
0.85V
TPS82085SIL, U12
0.85V, Max 3A
0.85V
TPS82085SIL, U13
1.8V, Max 3A
1.8V
TPS82085SIL, U24
0.9V, Max 3A
0.9V
TPS82085SIL, U15
1.1V, Max 3A
1.1V
TPS3106K33, U19
3.3V, Max 10mA
3.3V

Power Distribution

Power-On Sequence



Power Sequency

Power Rails

Power Rail Name	B2B Connector JM1 Pin	B2B Connector JM2 Pin	B2B Connector JM3 Pin	Direction	Notes
VIN	1, 3, 5	2, 4, 6, 8	Input	Supply voltage from the carrier board	
3.3V	-	10, 12	Output	Internal 3.3V voltage level	
3.3VIN	13, 15	-	Input	Supply voltage from the carrier board	
1.8V	39	-	Output	Internal 1.8V voltage level	
JTAG VREF	-	91	Output	JTAG reference voltage. Attention: Net name on schematic is "3.3VIN"	
VCCO_64	-	7, 9	Input	High performance I/O bank voltage	
VCCO_65	-	5	Input	High performance I/O bank voltage	
VCCO_66	9, 11	-	Input	High performance I/O bank voltage	

Module power rails.

Bank Voltages

Bank	Schematic Name	Voltage	Notes
24 HD	VCCO_HD24_24	Variable	Max voltage 3.3V
25 HD		Variable	Max voltage 3.3V
26 HD	VCCO_HD25_26	Variable	Max voltage 3.3V
44 HD	VCCO_HD24_44	Variable	Max voltage 3.3V
65 HP	VCCO_65	Variable	Max voltage 1.8V
66 HP	VCCO_66	1.8V	
500 PSMIO	VCCO_PSIO0_500	1.8V	
501 PSMIO	VCCO_PSIO1_501	3.3V	
502 PSMIO	VCCO_PSIO2_502	1.8V	
503 PSCONFIG	VCCO_PSIO3_503	1.8V	
504 PSDDR	DDR_1V2	1.2V	

Zynq SoC bank voltages.

Board to Board Connectors

These connectors are hermaphroditic. Odd pin numbers on the module are connected to even pin numbers on the baseboard and vice versa.

4 x 5 modules use two or three Samtec Razor Beam LSHM connectors on the bottom side.

- 2 x REF-189016-02 (compatible to LSHM-150-04.0-L-DV-A-S-K-TR), (100 pins, "50" per row)
- 1 x REF-189017-02 (compatible to LSHM-130-04.0-L-DV-A-S-K-TR), (60 pins, "30" per row) (depending on module)

Connector Mating height

When using the same type on baseboard, the mating height is 8mm. Other mating heights are possible by using connectors with a different height

Order number	Connector on baseboard	compatible to	Mating height
23836	REF-189016-01	LSHM-150-02.5-L-DV-A-S-K-TR	6.5 mm
	LSHM-150-03.0-L-DV-A-S-K-TR	LSHM-150-03.0-L-DV-A-S-K-TR	7.0 mm
23838	REF-189016-02	LSHM-150-04.0-L-DV-A-S-K-TR	8.0 mm
	LSHM-150-06.0-L-DV-A-S-K-TR	LSHM-150-06.0-L-DV-A-S-K-TR	10.0mm
26125	REF-189017-01	LSHM-130-02.5-L-DV-A-S-K-TR	6.5 mm
	LSHM-130-03.0-L-DV-A-S-K-TR	LSHM-130-03.0-L-DV-A-S-K-TR	7.0 mm
24903	REF-189017-02	LSHM-130-04.0-L-DV-A-S-K-TR	8.0 mm
	LSHM-130-06.0-L-DV-A-S-K-TR	LSHM-130-06.0-L-DV-A-S-K-TR	10.0mm

Connectors.

The module can be manufactured using other connectors upon request.

Connector Speed Ratings

The LSHM connector speed rating depends on the stacking height; please see the following table:

Stacking height	Speed rating
12 mm, Single-Ended	7.5 GHz / 15 Gbps
12 mm, Differential	6.5 GHz / 13 Gbps
5 mm, Single-Ended	11.5 GHz / 23 Gbps
5 mm, Differential	7.0 GHz / 14 Gbps

Speed rating.

Current Rating

Current rating of Samtec Razor Beam™ LSHM B2B connectors is 2.0A per pin (2 adjacent pins powered).

Connector Mechanical Ratings

- Shock: 100G, 6 ms Sine
- Vibration: 7.5G random, 2 hours per axis, 3 axes total

Manufacturer Documentation

File	Modified
PDF File hsc-report_lshm-lshm-05mm_web.pdf High speed test report	07 04, 2016 by Thorsten Trenz
PDF File lshm_dv.pdf LSHM catalog page	07 04, 2016 by Thorsten Trenz
PDF File LSHM-1XX-XX.X-X-DV-A-X-X-TR-FOOTPRINT(1).pdf Recommended layout and stencil drawing	07 04, 2016 by Thorsten Trenz
PDF File LSHM-1XX-XX.X-XX-DV-A-X-X-TR-MKT.pdf Technical drawing	07 04, 2016 by Thorsten Trenz
PDF File REF-189016-01.pdf Technical Drawing	07 04, 2016 by Thorsten Trenz
PDF File REF-189016-02.pdf Technical Drawing	07 04, 2016 by Thorsten Trenz

PDF File REF-189017-01.pdf Technical Drawing	07 04, 2016 by Thorsten Trenz
PDF File REF-189017-02.pdf Technical Drawing	07 04, 2016 by Thorsten Trenz
PDF File TC0923--2523_report_Rev_2_qua.pdf Design qualification test report	07 04, 2016 by Thorsten Trenz
PDF File tc0929--2611_qua(1).pdf Shock and vibration report	07 04, 2016 by Thorsten Trenz

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Technical Specifications

Absolute Maximum Ratings

Symbols	Description	Min	Max	Unit
VIN supply voltage	-0.3	7	V	See EN6347QI and TPS82085SIL datasheets
3.3VIN supply voltage	-0.1	3.630	V	Xilinx DS925 and TPS27082L datasheet
PS I/O supply voltage, VCCO_PSIO	-0.5	3.630	V	Xilinx document DS925
PS I/O input voltage	-0.5	VCCO_PSIO + 0.55	V	Xilinx document DS925
HP I/O bank supply voltage, VCCO	-0.5	2.0	V	Xilinx document DS925
HP I/O bank input voltage	-0.55	VCCO + 0.55	V	Xilinx document DS925
PS GTR reference clocks absolute input voltage	-0.5	1.1	V	Xilinx document DS925
PS GTR absolute input voltage	-0.5	1.1	V	Xilinx document DS925
Voltage on SC CPLD pins	-0.5	3.75	V	Lattice Semiconductor MachXO2 datasheet
Storage temperature	-40	+85	°C	See eMMC datasheet

PS absolute maximum ratings

Recommended Operating Conditions

Operating temperature range depends also on customer design and cooling solution. Please contact us for options.

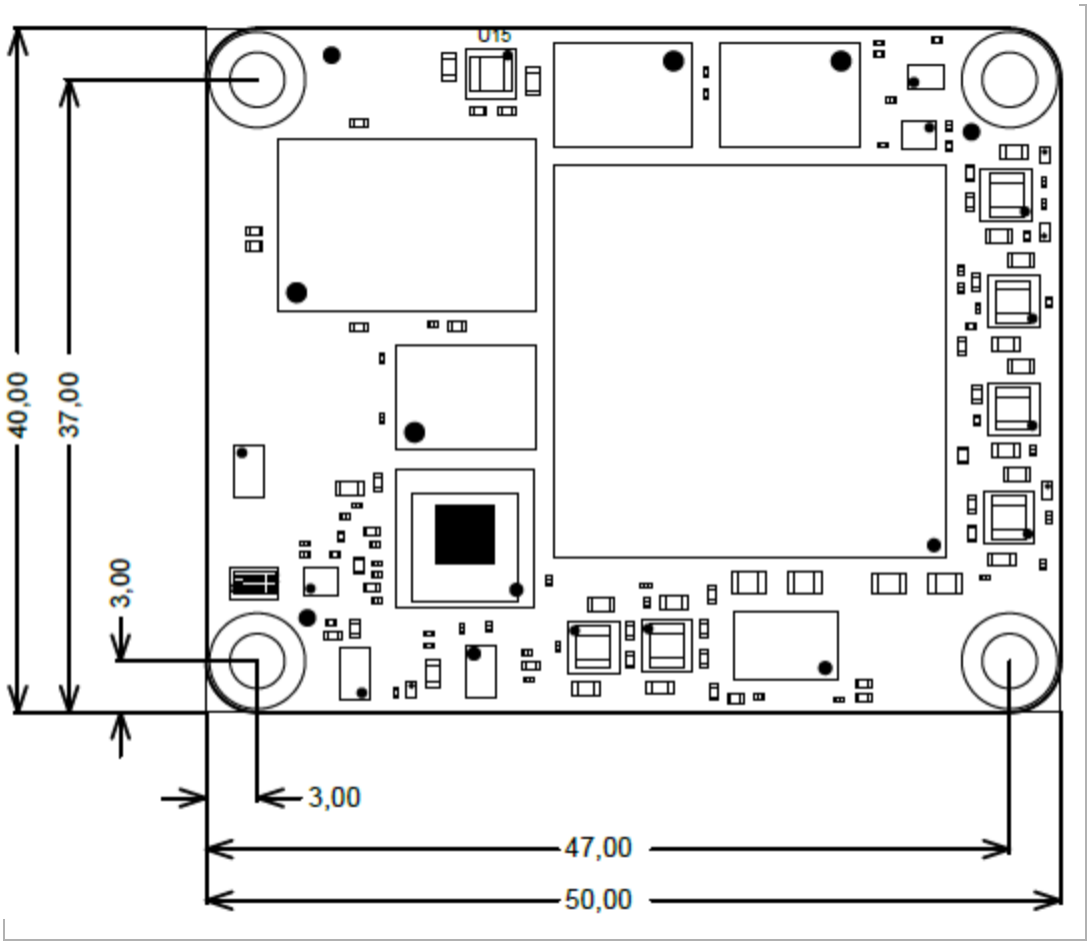
Parameter	Min	Max	Units	Reference Document
VIN supply voltage	3.3	6	V	See TPS82085S datasheet
3.3VIN supply voltage	3.3	3.465	V	See LCMXO2-256HC, Xilinx DS925 datasheet
PS I/O supply voltage, VCCO_PSIO	1.710	3.465	V	Xilinx document DS925
PS I/O input voltage	–0.20	VCCO_PSIO + 0.20	V	Xilinx document DS925
HP I/O banks supply voltage, VCCO	0.950	1.9	V	Xilinx document DS925
HP I/O banks input voltage	-0.20	VCCO + 0.20	V	Xilinx document DS925
Voltage on SC CPLD pins	-0.3	3.6	V	Lattice Semiconductor MachXO2 datasheet
Operating Temperature Range	0	85	°C	Xilinx document DS925, extended grade Zynq temperarure range

Recommended operating conditions.

Physical Dimensions

- Module size: 40 mm × 50 mm. Please download the assembly diagram for exact numbers.
- Mating height with standard connectors: 8 mm.

PCB thickness: 1.7 mm.



Physical Dimension

Currently Offered Variants

Trenz shop TE0823 overview page	
English page	German page

Trenz Electronic Shop Overview

Revision History

Hardware Revision History

Date	Revision	Changes	Documentation Link
2018-09-25	REV01	Initial Release	REV01

Hardware Revision History

Hardware revision number can be found on the PCB board together with the module model number separated by the dash.

Board hardware revision number.

Document Change History

Date	Revision	Contributor	Description

Error rendering macro 'page-info' Ambiguous method overloading for method jdk.proxy279.$Proxy4022#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]	**Error rendering macro 'page-info'** Ambiguous method overloading for method jdk.proxy279.$Proxy4022#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]	**Error rendering macro 'page-info'** Ambiguous method overloading for method jdk.proxy279.$Proxy4022#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]	• Bugfix document style
2021-08-23	v.42	Pedram Babakhani	• Bugfix Boot mode
2020-11-02	v.40	Pedram Babakhani	• Initial Release

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Document change history.

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Please also note our data protection declaration at https://www.trenz-electronic.de/en/Data-protection-Privacy

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To confront directly with the responsibility toward the environment, the global community and eventually also oneself. Such a resolution should be integral part not only of everybody's life. Also enterprises shall be conscious of their social responsibility and contribute to the preservation of our common living space. That is why Trenz Electronic invests in the protection of our Environment.

REACH, RoHS and WEEE

REACH

Trenz Electronic is a manufacturer and a distributor of electronic products. It is therefore a so called downstream user in the sense of REACH. The products we supply to you are solely non-chemical products (goods). Moreover and under normal and reasonably foreseeable circumstances of application, the goods supplied to you shall not release any substance. For that, Trenz Electronic is obliged to neither register nor to provide safety data sheet. According to present knowledge and to best of our knowledge, no SVHC (Substances of Very High Concern) on the Candidate List are contained in our products. Furthermore, we will immediately and unsolicited inform our customers in compliance with REACH - Article 33 if any substance present in our goods (above a concentration of 0,1 % weight by weight) will be classified as SVHC by the European Chemicals Agency (ECHA).

RoHS

Trenz Electronic GmbH herewith declares that all its products are developed, manufactured and distributed RoHS compliant.

WEEE

Information for users within the European Union in accordance with Directive 2002/96/EC of the European Parliament and of the Council of 27 January 2003 on waste electrical and electronic equipment (WEEE).

Users of electrical and electronic equipment in private households are required not to dispose of waste electrical and electronic equipment as unsorted municipal waste and to collect such waste electrical and electronic equipment separately. By the 13 August 2005, Member States shall have ensured that systems are set up allowing final holders and distributors to return waste electrical and electronic equipment at least free of charge. Member States shall ensure the availability and accessibility of the necessary collection facilities. Separate collection is the precondition to ensure specific treatment and recycling of waste electrical and electronic equipment and is necessary to achieve the chosen level of protection of human health and the environment in the European Union. Consumers have to actively contribute to the success of such collection and the return of waste electrical and electronic equipment. Presence of hazardous substances in electrical and electronic equipment results in potential effects on the environment and human health. The symbol consisting of the crossed-out wheeled bin indicates separate collection for waste electrical and electronic equipment.

Trenz Electronic is registered under WEEE-Reg.-Nr. DE97922676.

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