

# TEB0707 CPLD Firmware

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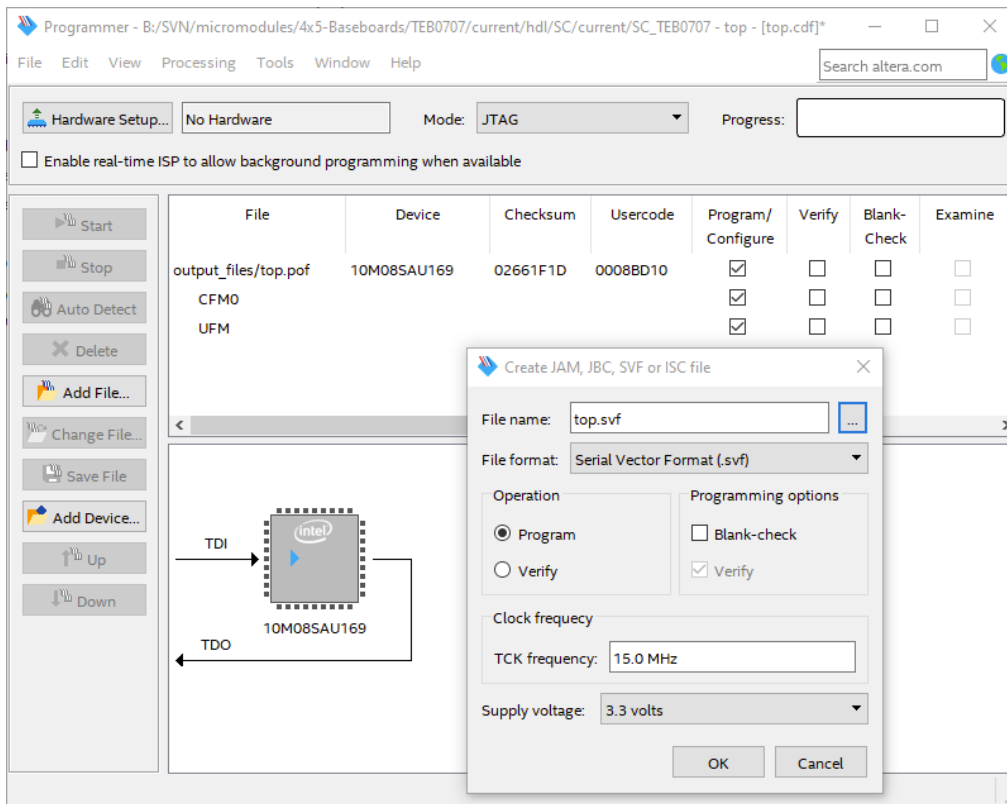
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## Available CPLD Firmware

- [TEB0707 SC CPLD](#) - Firmware description
  - Default delivered Firmware

## CPLD Access and Programming

1. Connect micro USB to PC.
2. Connect 5V Power supply.
3. Select CPLD JTAG by putting dip switch S1-4 in position ON.
4. Export Serial Vector Format File (SVF)
  - a. Open Project in Quartus Programmer
  - b. make sure pof file is selected for programming, if not remove sof file and add pof file.
  - c. Go to menu: "File" "Create JAM, JBC, SVF or ISC File..."
  - d. Select File format svf.
  - e. Set TCK Frequenzy to 15 MHz.
  - f. Export by clicking OK. If no other location was defined, the gernerated file is in the project folder.



Use MBFTDI SVF Player <https://github.com/marsohod4you/MBFTDI-SVF-Player>

1. Sources and precompiled binaries are available. Download precompiled binary (mbftdi.exe) and save in the folder where your svf file is located.
2. Close all programs which may connect to the used usb port (Quartus, Vivado/Vitis, Putty etc ...)
3. Open Windows CMD and go to folder where svf file is located.
4. Start Programming by typing: "mbftdi.exe top.svf" where top.svf is the exported svf file. Successful programming looks like:

```
d:/mbftdi.exe top.svf
mbftdi v1.4 - burn MAX2 CPLD from Altera Vector Programming File *.svf
FTDI port to JTAG is used for programming
Usage example: mbftdi myfile.svf
```

```
Checking for FTDI devices...
2 FTDI devices found - the count includes individual ports on a single chip
Assume first device has the MPSSE and open it...
Device: Digilent Adept USB Device A
Serial: 405436310724A
Hi-speed device (FT232H, FT2232H or FT4232H) detected
Configuring port for MPSSE use...
Frequency is set to 15MHz (FTDI clk divider 0001), required 15MHz
```

```
JTAG program executed successfully.
Press <Enter> to continue
```

