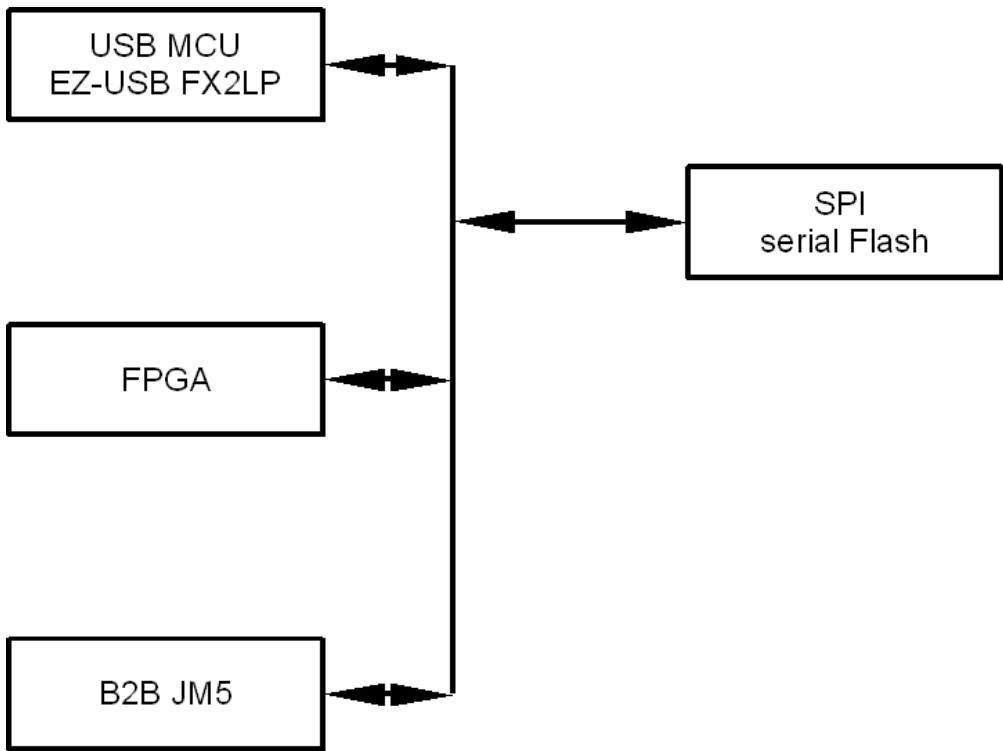


TE0320 SPI Interface

TE0320 has a flexible SPI bus on-board as outlined in the figure below.



SPI bus topology.

SPI signals on the TE0320 are listed and described in the table below.


na me	definition	description
SPI_Q	serial data output	This output signal is used to transfer data serially out of the device. Data is shifted out on the falling edge of SPI_/C.
SPI_D	serial data input	This input signal is used to transfer data serially into the device. It receives instructions, addresses, and the data to be programmed. Values are latched on the rising edge of SPI_/C
SPI_/C	serial clock	This input signal provides the timing of the serial interface. Instructions, addresses, or data present at SPI_D are latched on the rising edge of SPI_/C. Data on SPI_Q changes after the falling edge of SPI_/C.
SPI_/S	chip select	When this input signal is high , the device is disabled and SPI_Q is at high impedance (Z).
		When this input signal is low , the device is enabled .
		After power-up, a falling edge on SPI_/S is required prior to the start of any instruction to the Flash memory.

SPI signals summary.


SPI signal pin-out of the TE0320 is summarized in the table below.

name	FPGA ball	JM5 pin
SPI_Q	AF24	18
SPI_D	AB15	12
SPI_/C	AE24	22
SPI_/S	AA7	20

SPI pin-out summary.

 SPI pins on B2B connector JM5 cannot be used as GPIOs (general purpose I/Os).

The SPI bus can be used during configuration and operation in a plurality of ways as summarized respectively in Table A (SPI bus for configuration) and Table B (SPI bus for operation).

 Any other usage of the SPI bus is neither supported nor recommended.

SPI bus for configuration

The SPI bus is used for configuration in two ways by default:

1. EZ-USB \hat{a} -Flash the USB FX2 microcontroller (master) writes the PROM file (containing the FPGA configuration bitstream) to the SPI serial Flash memory (slave)
2. FPGA \hat{a} —, Flash the FPGA (master) configures itself in Master SPI mode from the SPI serial Flash memory (slave).

In case (a), the FPGA shall be turned off to release its shared SPI pins.

In case (b), the USB FX2 microcontroller shall three-state (Z = high impedance) its shared SPI pins.

description	usage	EZ-USB FX2LP	FPGA	B2B JM5	serial Flash
EZ-USB \hat{a} -Flash	OpenFU T API	master	off (S2 = FX2PON, FX2_PS_EN = 0)	deselected	slave
FPGA \hat{a} —, Flash	OpenFU T API	inactive SPI_* = Z	master (SPI_/S = 1)	deselected	slave
B2B JM5 \hat{a} -Flash	custom	inactive SPI_* = Z	off (S2 = FX2PON, FX2_PS_EN = 0)	master (SPI_/S = 0)	slave

Table A: SPI bus modes for configuration.

The PROM file (containing the FPGA configuration bitstream) can be written to the SPI serial Flash memory (slave) also through the SPI pins of B2B connector JM5 (attached device set to master mode). In this case, the FPGA shall be turned off or three-stated to release its shared SPI pins and the USB FX2 microcontroller shall three-state (Z = high impedance) its shared SPI pins.

SPI bus for operation

A plurality of usage combinations of the SPI bus during operation is made available to the user as suggested in Table B below.

description	usage	EZ-USB FX2LP	FPGA	B2B JM5	serial Flash
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EZ-USB \hat{a} Flash	custom	master	off (S2 = FX2PON, FX2_PS_EN = 0)	deselected	slave
FPGA \hat{a} Flash	custom	inactive SPI_* = Z	master (SPI_/S = 1)	deselected	slave
B2B JM5 \hat{a} Flash	custom	inactive SPI_* = Z	off (S2 = FX2PON, FX2_PS_EN = 0)	master (SPI_/S = 0)	slave
EZ-USB \hat{a} B2B JM5	custom	master SPI_/S = 1	off (S2 = FX2PON, FX2_PS_EN = 0)	slave	deselected
EZ-USB \hat{a} B2B JM5	custom	slave SPI_/C = Z	off (S2 = FX2PON, FX2_PS_EN = 0)	master (SPI_/S = 1)	deselected

Table B: SPI bus modes for operation.



Other combinations of master and slave units are neither supported nor recommended.