## TE0320 DIP Slide Switches S5[A:H] (User)

TE0320 is provided with 8 user DIP slide switches as shown in the figure below: S5A to S5H.


DIP slide switches S5[A:H].
Please note the 8 switch labels are on one side and the <ON> label is on the opposite side. DIP slide switches $\mathrm{S} 5[\mathrm{~A}: \mathrm{H}]$ condition the value of some user signals as described in the table below.

| switch | S5 label | signal name | FPGA <br> ball | FPGA pin | FPGA <br> bank |
| :---: | :---: | :---: | :---: | :---: | :---: |
| S5A | 1 | US1 | F24 | IO_L54N_1 | 1 |
| S5B | 2 | US2 | E24 | IO_L56P_1 | 1 |
| S5C | 3 | US3 | E26 | IO_L60P_1 | 1 |
| S5D | 4 | US4 | D24 | IO_L61N_1 | 1 |
| S5E | 5 | US5 | D26 | IO_L60N_1 | 1 |
| S5F | 6 | US6 | D25 | $10 . L 61 P_{-} 1$ | 1 |
| S5G | 7 | US7 | C26 | $\begin{aligned} & \text { IO_L63P_1 } \\ & \text { A22 } \end{aligned}$ | 1 |
| S5H | 8 | US8 | C25 | $\begin{aligned} & \text { IO_L63N_1 } \\ & \text { A23 } \end{aligned}$ | 1 |

S5X settings description.
A signal listed in the table above is set low (logical 0 ) when a slide switch is set to <ON>, and vice-versa.

