

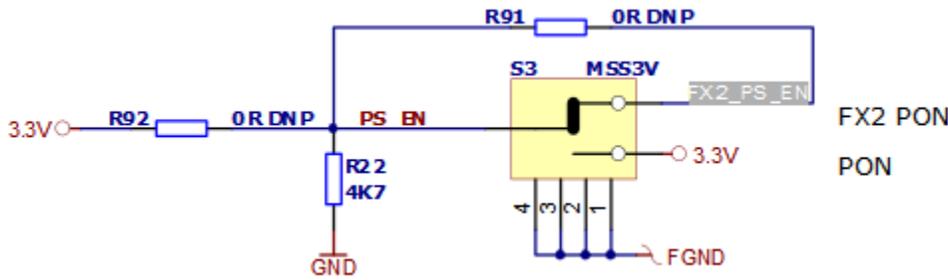
TE0300 DIP Slide Switch S3 (Configuration)

TE0300 is provided with a slide switch S3.
 Slide switch S3 conditions the value of signal PS_EN.
 In this way, S3 conditionally/unconditionally enables the power rails 1.2 V and 2.5 V.

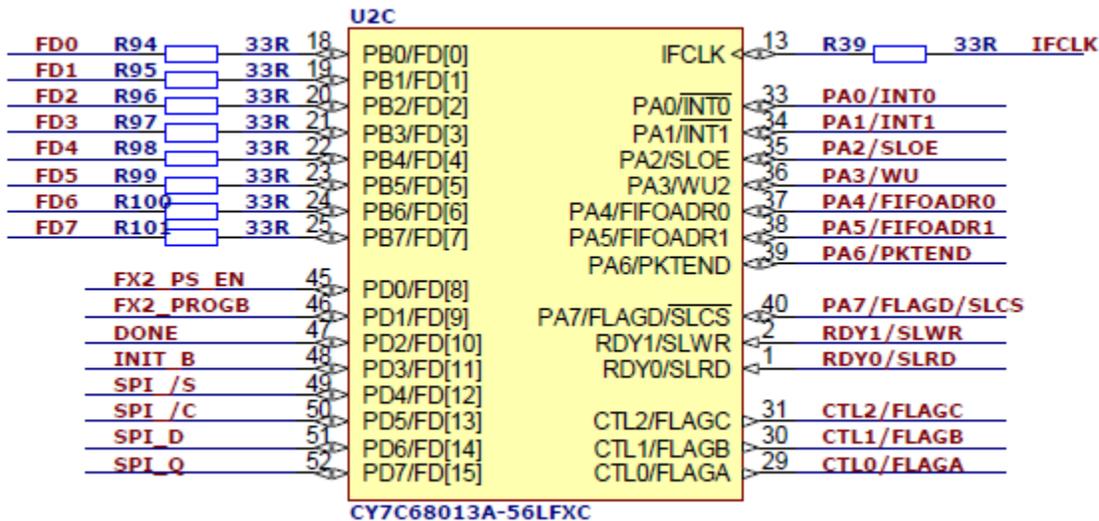
✔ Note. DNP: Do Not Populate aka Do Not Solder the Component associated to DNP label.



Slide switch S3 (angle view)



Slide switch S3 schematic



When slide switch S3 = FX2 PON, signal PS_EN is set to signal FX2_PS_EN driven by the EZ-USB FX2LP USB FX2 microcontroller under user control.

When S3 is turned **on (closed, FX2 PON)**, the power rails 1.2 V and 2.5 V are controlled by the USB (EZ-USB FX2LP USB FX2) microcontroller. At start-up, the USB microcontroller switches off the power rails 1.2 V and 2.5 V and starts up the module in low-power mode. After enumeration, the USB microcontroller firmware enables (switches on) the power rails 1.2 V and 2.5 V, if enough current is available from the USB bus.

When S3 is turned **off (open, PON)**, the power rails 1.2 V and 2.5 V are always enabled (switched on).

 When S3 is turned on (*FX2 PON*), make sure that no signals are applied to the input pins when power-rails are disabled by the USB microcontroller (at start-up).

S3 position	Default position	Effect on 1.2 V and 2.5 V power rails
FX2 PON (on, closed)	✔	1.2 V and 2.5 V rails controlled by USB FX2 microcontroller (signal FX2_PS_EN) PS_EN = FX2_PS_EN = 1 or 0
PON (off, open)	✘	1.2 V and 2.5 V rails always enabled (PS_EN = 1) PS_EN FX_PS_EN = 1 or 0

Slide switch S3 settings overview (power rails 1.2 V and 2.5 V only)

Signal FX2_PS_EN

To command signal **FX2_PS_EN**, read the [reference firmware code](#).

IOD = 0x03; // Enable PS_EN and disable PROG_B

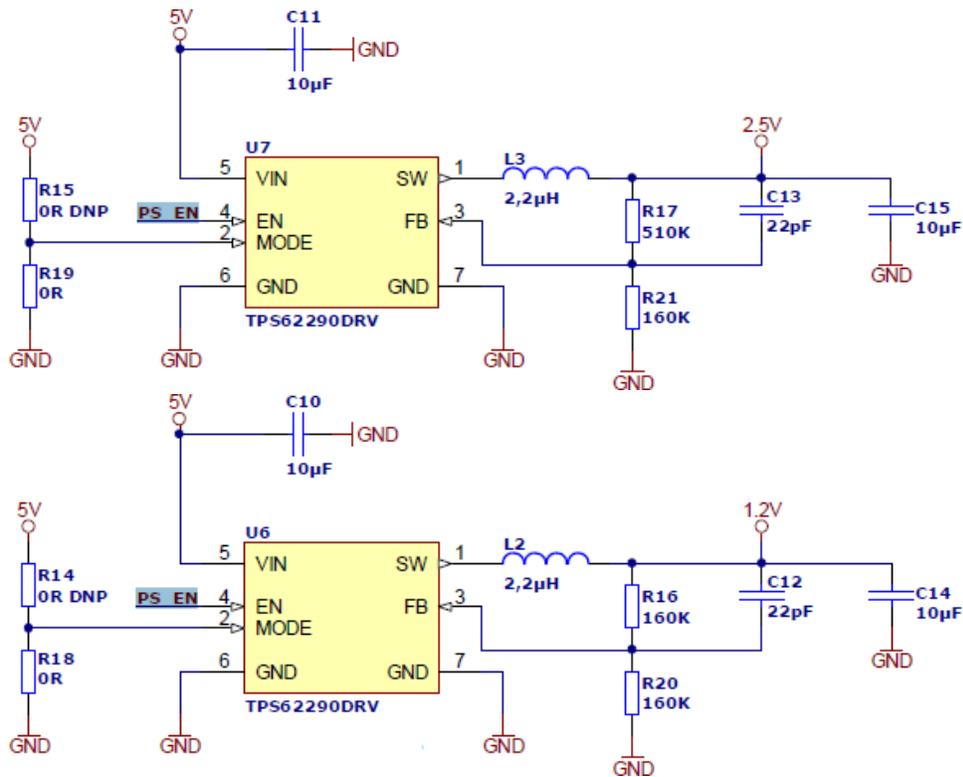
OED = 0x03; // Configure PS_EN and PROG as outputs

Port D Pin	Alternate Function	Alternate Function is Selected By...	Alternate Function is Described in...
PD.7:0	FD[15:8]	IFCFG1 = 1 and any WORDWIIDE bit = 1	Slave FIFOs chapter 9 on page 99

Table from **EZ-USB(R) Technical Reference Manual (EZ-USB_TRM.pdf)**.
USB FX2 microcontroller configuration table

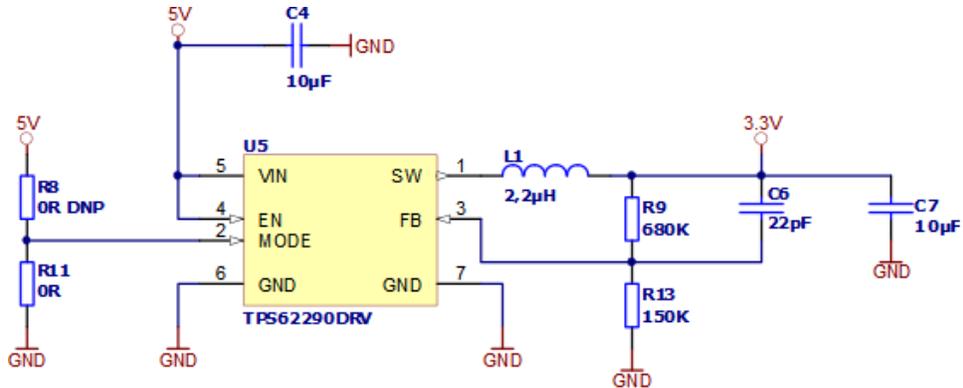
Signal PS_EN

- Signal PS_EN enables (1) or disables (0) power rails 1.2 V and 2.5 V.



Power rails 1.2 V and 2.5 V could be enabled/disabled by signal PS_EN

- Power-rail 3.3V is not controlled by signal PS_EN and is unconditionally enabled. The power-rail 3.3 V though is out of the control of the USB-microcontroller and is supplied down-converting the power supply 5 V provided by either the USB-bus or the B2B receptacle connector. In this case, signals that are applied to the 3.3 V I/O banks do not need to be disconnected when power-rails are disabled by the USB microcontroller.



Power rail 3.3V could not be enabled/disabled by signal PS_EN

VCCIO0 assembly options

According to the corresponding assembly option, power rail VCCCI00 can depend or not on the power rail 2.5V.

Voltage VccIO for bank B0 shall span from 1.2 V to 3.3 V. VccIO can be supplied either externally or internally to the micromodule.

Warning! Spartan-3 I/Os are not 5 V tolerant. Applying more than the recommended operating voltages at any pin, results in a damaged FPGA (see [Xilinx Answer AR#19146](#)).

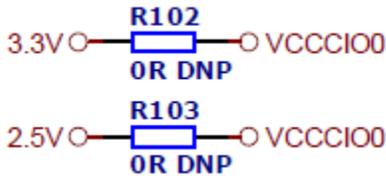
Externally Supplied VCCIO

VccIO can be externally supplied over the B2B connector J4. If bank B0 is not used, then VccIO can be left open.

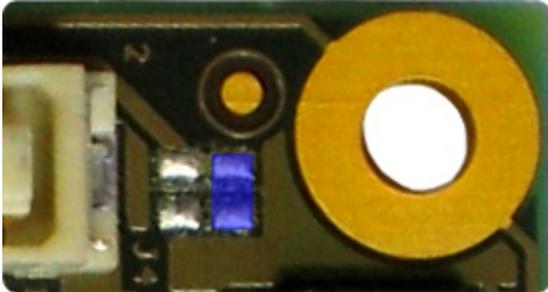
Internally Supplied VCCIO

If VccIO is **not** externally supplied, it can be internally supplied by **one** of the internal power rails of 2.5 V and 3.3 V. This is possible by short-circuiting **one** of the two pad pairs placed on the right of connector J4 at the top right corner of the bottom side of the micromodule.

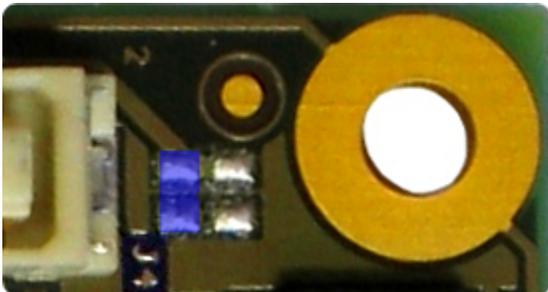
Two suitable ways of short-circuiting the pad pair are by means of a zero-ohm 0603 (1608 metric) chip resistor or a solder blob.



The soldering of R102 and R103 are mutually exclusive.



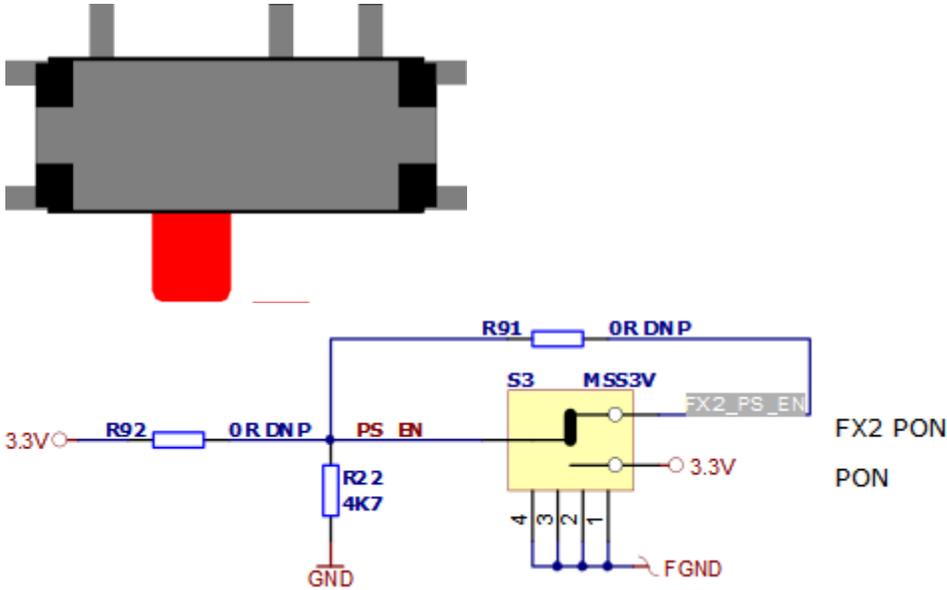
The figure shows how to short-circuit VccIO to internal power rail 3.3 V. FX2_PS_EN does not control VCCCI00 (3.3V) FPGA bank 0



The figure shows how to short-circuit VccIO to internal power rail 2.5 V. FX2_PS_EN does control VCCCI00 (2.5V) FPGA bank 0

Slide Switch S3 = FX2 PON

When slide switch **S3** is in the **left position** (= **FX2 PON** : power rails conditionally on depending on signal FX2_PS_EN), signal **PS_EN** is set to signal **FX2_PS_EN** (**PS_EN = FX2_PS_EN**) driven by the EZ-USB FX2LP USB FX2 microcontroller under user control (**IOD** and **OED** of **fw.c**).

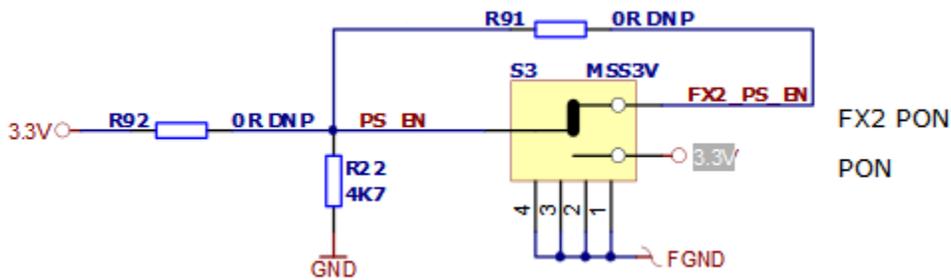
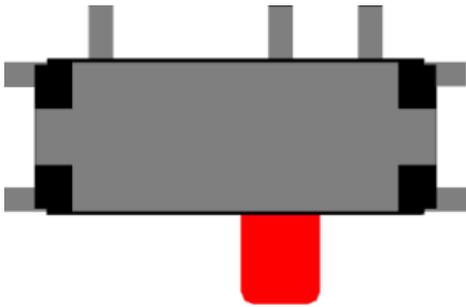


S3 on position FX2 PON (PS_EN = FX2_PS_EN = 1 or 0).

1. Dynamic **full power** operation (**PS_EN = 1**): when the EZ-USB FX2LP USB FX2 microcontroller sets signal **PS_EN = FX2_PS_EN = 1**, power rails 1.2 V and 2.5 V are enabled.
This setting can be useful for .
2. Dynamic **low power** operation (**PS_EN = 0**): when the EZ-USB FX2LP USB FX2 microcontroller resets signal **PS_EN = FX2_PS_EN = 0**, the following components are switched off:
 - FPGA core logic (1.2V)
 - DDR SDRAM (2.5V)
 - FPGA bank 1 (2.5V)
 - VREF (2.5V)
 - VCCIO0 (2.5V) FPGA bank 0 (if R102+R103- assembly)

Slide Switch S3 = PON

Full power operation (**PS_EN = 1**): when slide switch S3 is in the right position (PON = power rails unconditionally on), signal PS_EN is set to power rail 3.3 V. Thus power rails 1.2 V and 2.5 V are unconditionally enabled.



S3 on position PON (PS_EN FX2_PS_EN = x; PS_EN = high).

Summary table

The table below summarizes all switching options implied by slide switch S3 and firmware signal FX2_PS_EN (under the standard assembly option).

power rail	S3= PON (PS_EN = 1) (PS_EN FX2_PS_EN) (Full power)	S3 = FX2 PON and PS_EN = FX2_PS_EN = 1 (Dynamic full power)	S3 = FX2 PON and PS_EN = FX2_PS_EN = 0 (Dynamic low power)
1.2V	on	on	off
2.5V	on	on	off
VCCCI00 (= 2.5V) R102+R103- assembly ⁽¹⁾	on	on	off
VCCCI00 (= 3.3V) R102-R103+ assembly ⁽²⁾	on	on	on

⁽¹⁾ R102 populated / R103 unpopulated

⁽²⁾ R102 unpopulated / R103 populated
Slide switch S3 settings overview (1.2V , 2.5V, VCCCI00).