TE0320 Power Supply

Power Supply Range

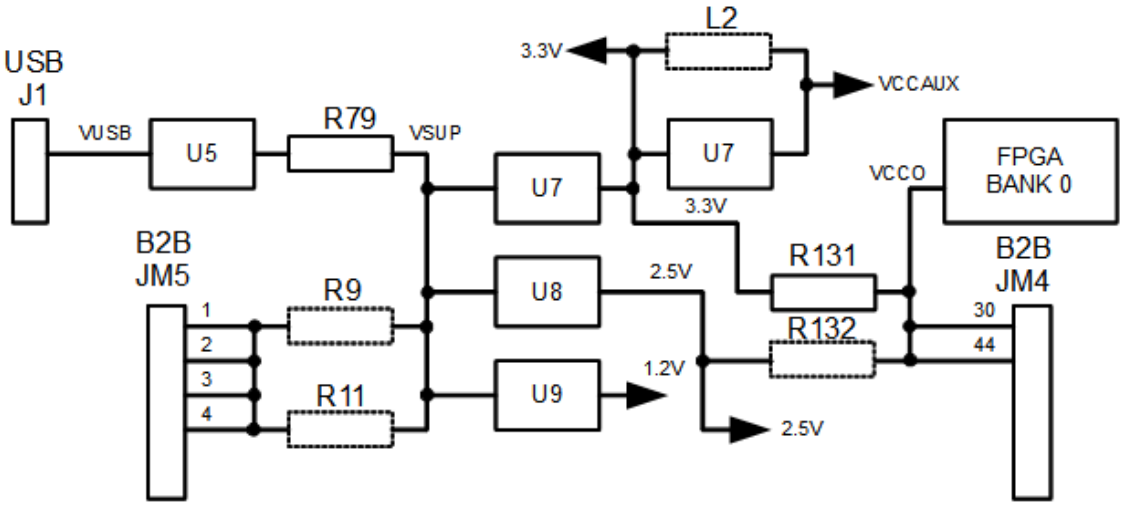
TE0320 requires only one power supply with a supply voltage between 4.0 V and 7.0 V. Power consumption depends on the active design.

Power Supply Sources

TE0320 can be power supplied in two ways:

- through USB connector J1,
- through B2B connector JM5 (pins 1 to 4).

The power supply source is determined by assembly option. See the figure below.



Power supply options diagram

1.2 V, 2.5 V and 3.3 V voltage rails are provided by corresponding step-down regulator DC/DC converters, each one capable of providing up to 3 A of output current. These three regulators are synchronized to switch with 120° phase lag, to improve EMC, and to reduce input ripple. The synchronization circuit can be omitted in cost sensitive applications (please contact Trenz Electronic).
Power supply inputs and outputs are made available at B2B connectors JM4 and JM5 for user applications.

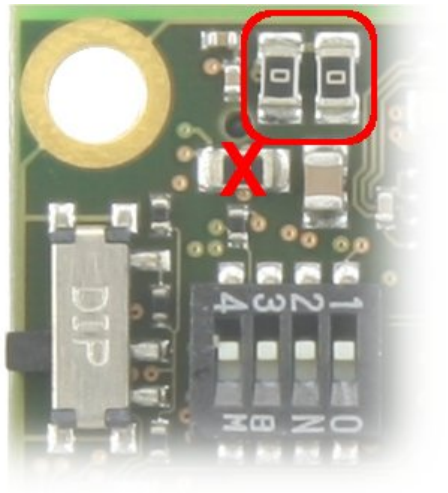
> Each pin of B2B connectors JM4 and JM5 is capable of a maximum current of 1.0 A.

power-rail name	nominal voltage (V)	maximum current (A)	power source	system supply	user supply
Vb2b	4.0 to 7.0	4.0 (4 pin × 1.0 $^{A}/_{pin}$)	JM5	module	-
Vusb	5.0	0.5	J1	module	-
Vsup	4.0 to 7.0	< 0.5	Vusb	3 × DC/DC DC/DC sync	JM5 (1.0 A)

		< 4	Vb2b	power-fail	
3.3V	3.3	3.0	Vsup â–º DC/DC	module	JM4 (1.0 A) JM5 (1.0 A)
2.5V	2.5	3.0	Vsup â–º DC/DC	DDR SDRAM	JM5 (1.0 A)
1.2V	1.2	3.0	Vsup â–º DC/DC	VCCINT	JM5 (1.0 A)
VCCAUX	2.5	0.3	3.3V â–º LDO	VCCAUX	JM4 (1.0 A)
	3.3	< 3.0	3.3V		
VCCCIO0	2.5	< 3.0	2.5V	VCCO (bank 0)	JM4 (1.0 A)
	3.3	< 3.0	3.3V		JM4 (1.0 A)
	1.10 to 3.60	2.0 (2 pin × 1.0 A/pin)	JM4 (30 + 44)		JM4 (30 / 44)

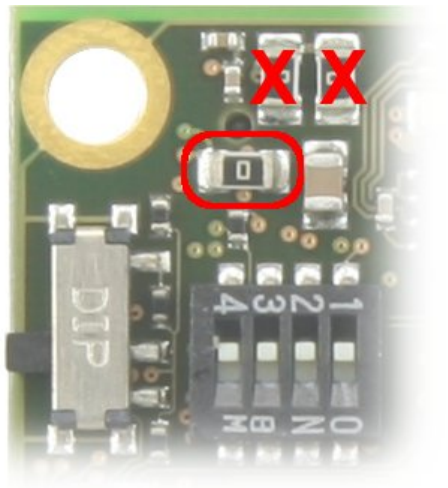
On-board power rails summary.

If resistors R9 and R11 are populated and R12 is not populated, then TE0320 is power supplied through JM5 (B2B connector).



Assembly combination for power supply through JM5.

If resistors R9 and R11 are not populated and R12 is populated, then TE0320 is power supplied through J1 (USB bus).



Assembly combination for power supply through J1.

> Any other assembly combination of R9, R11 and R12 is not allowed.

On Board Power Rails

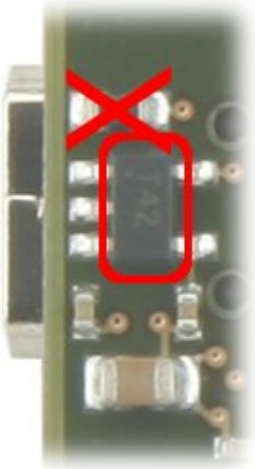
According to the Xilinx Spartan-3A DSP literature, there are the following power supply pin types:

- V_{CCAUX}: dedicated auxiliary power supply pins
- V_{CCINT}: dedicated internal core logic power supply pins
- V_{CCO}: supplies power to the output buffers within the I/O bank and sets the input threshold voltage for some I/O standards.

TE0320 has the following power rails on-board:

- Vsup
  It is the main internal power rail irrespective of the external power supply. It is supplied by either Vb2b or Vusb. It manages power distribution, conversion and supervision. It is routed also to connector JM5 as a user power supply output.
- Vb2b
  It is the main power rail when the module is supplied from B2B connector JM5.
- Vusb
  It is the main power rail when the module is supplied from USB mini-B connector J1. The maximum current than can be provided to J1 is determined by the USB power source.
- 3.3V
  It is converted from Vsup by a step-down DC/DC converter and can provide up to 3.0 A to the module and connectors JM4 and JM5.
- 2.5V
  It is converted from Vsup by a step-down DC/DC converter and can provide up to 3.0 A to the DDR SDRAM and connectors JM5.
- 1.2V
  It is converted from Vsup by a step-down DC/DC converter and can provide up to 3.0 A to the V_{CCINT} power supply pins and connectors JM5.
- VCCAUX
  Here there are two assembly options:

    a. if inductor L2 is not populated and the low-noise low drop-out regulator U6 is populated, VCCAUX power rail is supplied with its nominal voltage of 2.5 V. This is the recommended option for noise-sensitive circuitry such as clocking and timing infrastructures.



Assembly option for VCCAUX = 2.5 V (bottom view).

b. if the ferrite bead L2 is populated and U6 is not populated, the 3.3V power rail is simply filtered to generate VCCAUX power rail. This is the recommended option for cost-sensitive applications. In this case

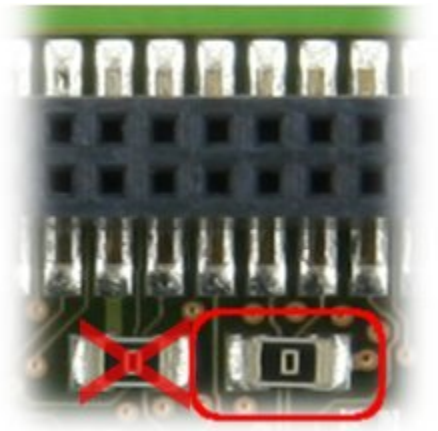
- ensure the noise level on power rail VCCUAX is suitable to your application;
- avoid the connection of noise sources to power rail VCCUAX.

Assembly option for VCCAUX = 3.3 V (bottom view).

> Any other assembly combination of L2 and U6 is not allowed.

- VCCCIO0
  VCCCIO0 supplies V_{CCO} to FPGA bank 0. The following assembly options are possible:

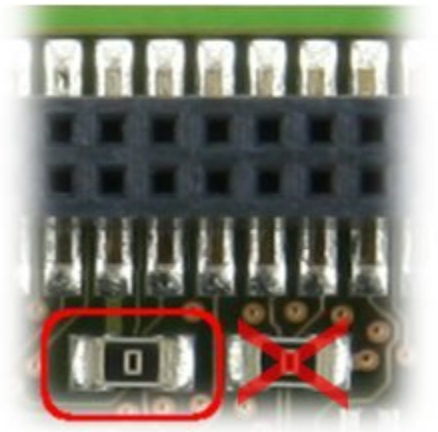
  a. if resistor R131 is not populated and R132 is populated, VCCCIO0 power rail is set to power rail 2.5V (nominal voltage = 2.5 V).



Assembly option for VCCIO0= 2.5 V (bottom view).

> ⚠ Pins 30 and 44 of JM4 are power supply **inputs** in this case.

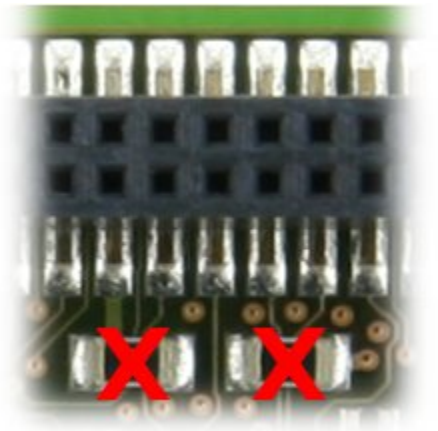
b. if resistor R131 is populated and R132 is not populated, VCCCIO0 power rail is set to power rail 3.3V (nominal voltage = 3.3 V). This is the default.



Assembly option for VCCCIO0 = 3.3 V (bottom view).

> ⚠ Pins 30 and 44 of JM4 are power supply **outputs** in this case.

c. if both resistors R131 and R132 are not populated, VCCCIO0 power can be supplied through pins 30 and 44 of B2B connector JM4.



Assembly option for VCCAUX = off (bottom view)

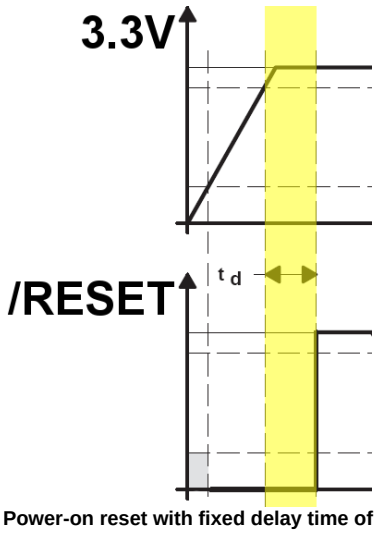
> ⚠ Pins 30 and 44 of JM4 are power supply **outputs** in this case.

> ⛔ Assembly option where both R131 and R132 are populated is not allowed.

Power Supervision

Power-on Reset

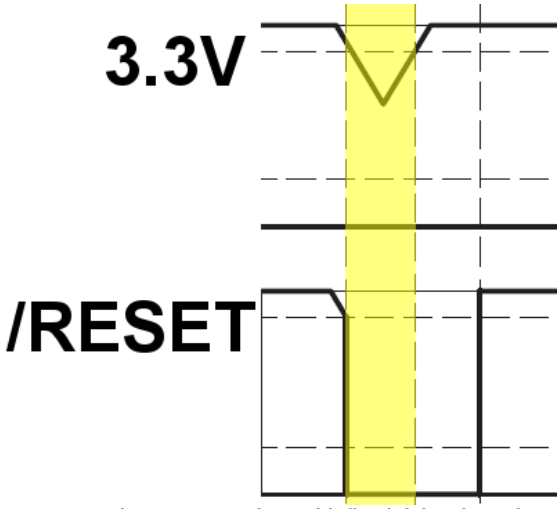
During power-on, the /RESET line is first asserted. Thereafter, the supply voltage supervisor monitors the power supply rail 3.3V and keeps the /RESET line active (low) as long as the rail remains below the threshold voltage (2.93 V). An internal timer delays the return of the /RESET line to the inactive state (high) to ensure proper system reset. The delay time of 200 ms starts after the rail has risen above the threshold voltage.



Power-on reset with fixed delay time of 200 ms

After this delay, the /RESET line is reset high and the FPGA configuration can start.

When the rail voltage drops below the threshold voltage, the /RESET line becomes active (low) again.



Reset assertion on power drop with fixed delay time of 200 ms.

Power-on Reset

TE0320 integrates a power-fail comparator which can be used for low-battery detection, power-fail warning, or for monitoring Vsup power rail.

An additional power-fail circuit can be used, to monitor the input voltage. At 4.4V, a power-fail signal (/PFO) is sent to the FPGA. Should you wish or need another threshold voltage, please contact Trenz Electronic.