

# TE USB FX2 Module Configuration

This section describes how to configure the TE USB FX2 module and access some of its resources.

To program the firmware in the EEPROM, the IIC bus should be correctly configured.

To program the bitstream in the Flash, the SPI bus should be correctly configured.

See the section [Switches: settings for USB Firmware, FPGA bitstream programming, Power Supply and reset](#).

See [Firmware and Bitstreams](#) for the files required.

TE USB FX2 modules can be configured through a host computer with the following system requirements:

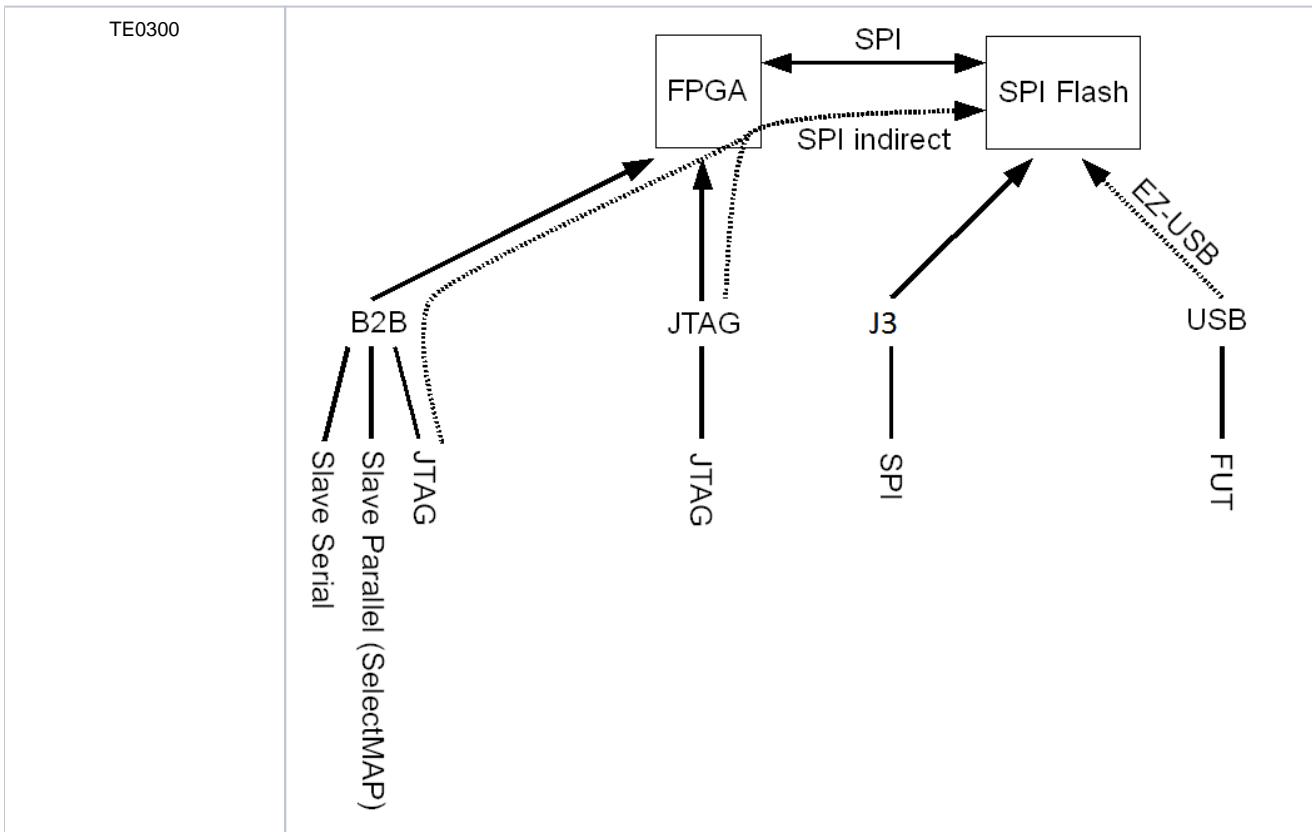
- Operating system: Microsoft Windows 2000, Microsoft Windows XP, Microsoft Vista, Microsoft Windows 7 or above;
- Xilinx ISE 10.1 or later for indirect SPI in-system programming (ISP) (for Spartan-3E aka TE0300, see [Xilinx Answer AR #25377](#));
- Xilinx EDK for some reference designs;
- Interface: USB host;
- JTAG cable with flying leads.
- SPI cable with flying leads (for TE0300) for direct SPI in-system programming (ISP).



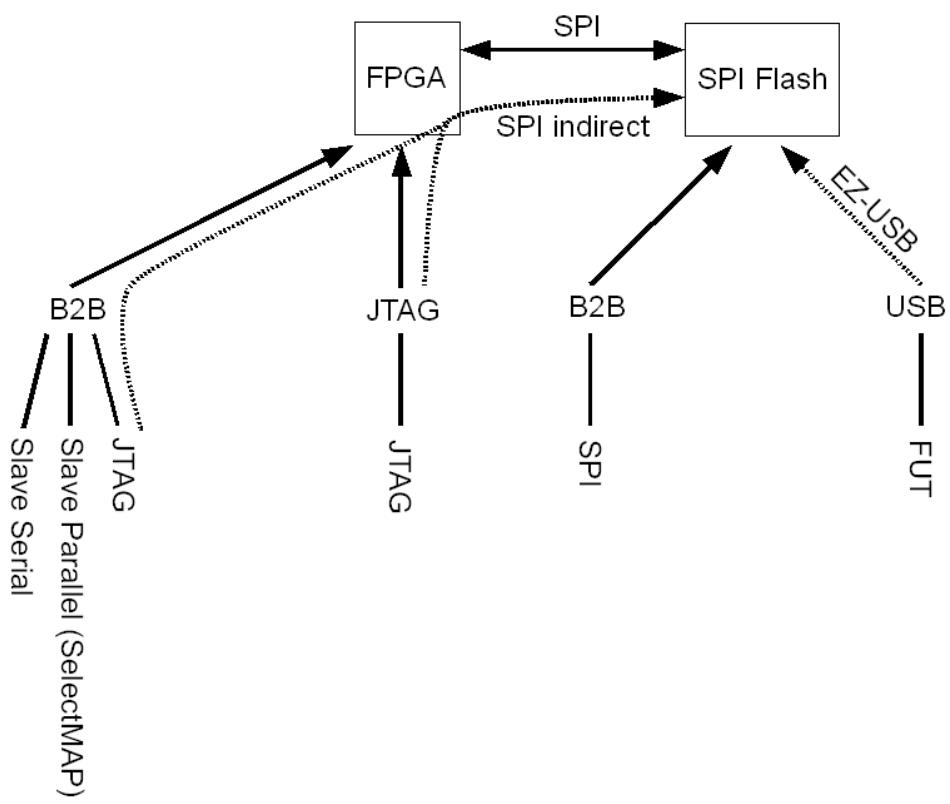
Direct SPI configuration is supported only up to Xilinx iMPACT version 11.x. See [Xilinx AR#36156](#). Available only for TE0300.

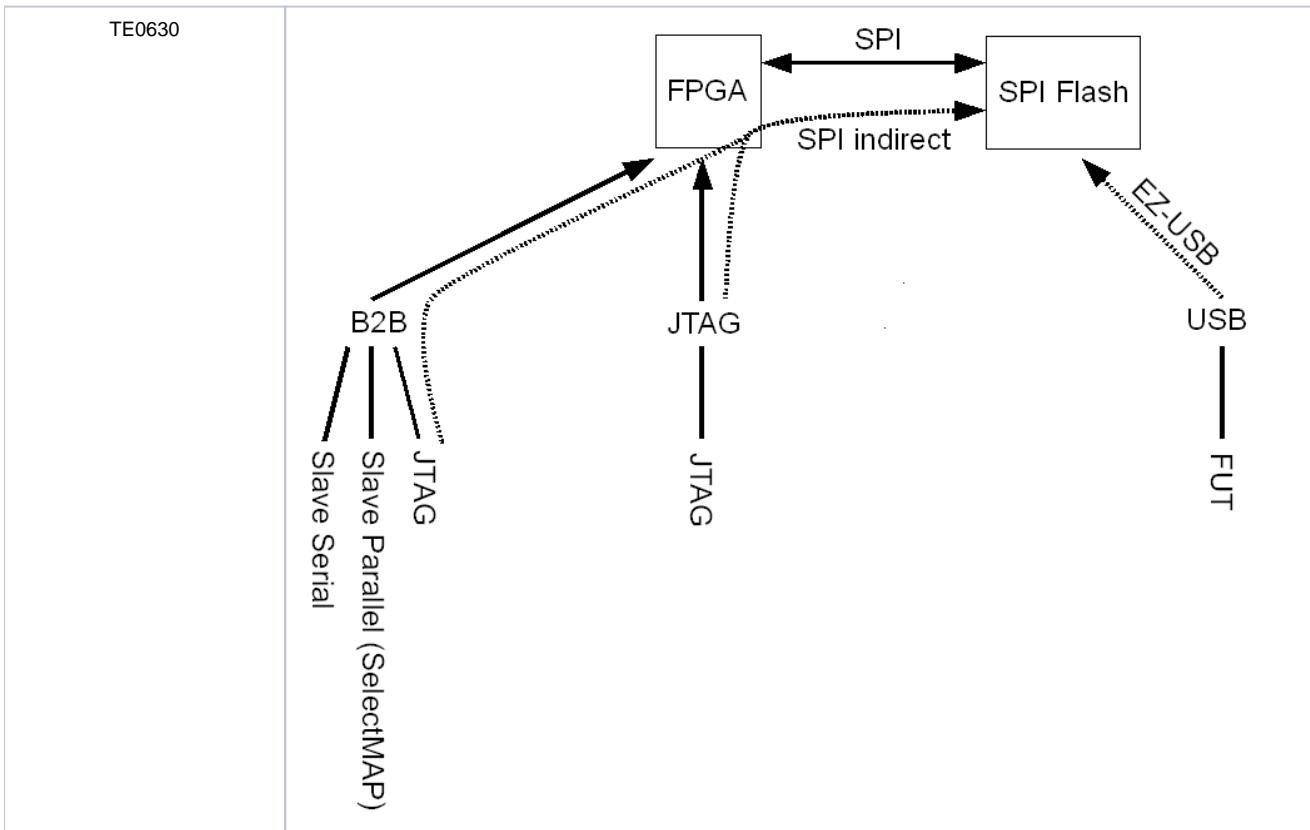
## Configuration mode connections available to the user

| TE USB FX2 module type | Configuration mode connections |
|------------------------|--------------------------------|
|------------------------|--------------------------------|



TE0320





Configuration modes overview: FPGA bitstream only.

## USB interface

TE USB FX2 module is equipped with a Cypress EZ-USB FX2 controller (TE USB FX2 microcontroller) to provide a high-speed USB 2.0 interface. Configuration of the TE USB FX2 module through a USB host is recommended for non-volatile on-site operations such as firmware upgrade or SPI Flash bitstream download.

Even when [USB connector](#) is used to program the FPGA image (aka FPGA bitstream), the SPI bus and the the SPI Flash memory are also used by C# [OpenFutNet](#) or [Python Open\\_FUT](#).



The procedure followed by one of the two TE programs (or by a custom user program) is the following:

- erase the SPI Flash ([FLASH\\_ERASE command](#));
- writes the bitstream image in the SPI Flash ([FLASH\\_WRITE command](#)) and readback the bytes written ([FLASH\\_READ command](#)) for integrity check;
- after SPI Flash writing is complete and checked, the FPGA is powered off ([POWER command](#) with command[1]=0) and then on ([POWER command](#) with command[1]=1);
- at power on the FPGA automatically read the SPI Flash content to configure itself;
- waits some seconds (2 to 10 seconds) the end of FPGA configuration; the FX2 microcontroller's firmware is able to read the DONE PIN status from PD2 pin (IOD2)
- a [READ\\_STATUS command](#) should be used to check if DONE PIN (reply[4] = EP1INBUF[4] = sts\_booting) is high (reply[4]=1) .

Even when [USB connector](#) is used to program the FX2 microcontroller's firmware, the IIC bus and the the IIC EEPROM memory are also used by C# [OpenFutNet](#) or [Python Open\\_FUT](#).

## Jtag Interface

The JTAG interface allows a

- fast (10 seconds), frequent but volatile configuration (only the FPGA is programmed using Xilinx ISE or EDK and a .bit bitstream and not the SPI Flash) of the TE USB FX2 module.
- medium-fast (1-2 minutes) non-volatile on-site operations such as SPI Flash bitstream download: [indirect SPI in-system programming \(ISP\)](#).

 Only through the JTAG interface it is possible to develop and debug with Xilinx tools (e.g. Xilinx SDK debug, Xilinx ChipScope, Xilinx Microprocessor Debugger).

## SPI Interface

SPI interfaces allows a medium-fast (1-2 minutes), frequent and non-volatile configuration (SPI Flash bitstream download) of the TE0300 module (through [J](#) and direct SPI programming or TE USB FX2 microcontroller and [OpenFutNet](#)), TE0320 module (through [B2B connection](#) or TE USB FX2 microcontroller and [OpenFutNet](#)), TE0630 module (through TE USB FX2 microcontroller and [OpenFutNet](#)).

## B2B Interface

Through B2B interface, the JTAG (all TE USB FX2 modules) bus or the SPI bus (TE0320 module only) could be used (see the two paragraphs above).

It is also possible to use B2B interface for

- Slave Parallel (SelectMAP) mode
- Slave Serial mode

This two mode need a microcontroller as intermediate to program/configure the FPGA.

## Interface Available to FX2 microcontroller

The FX2 microcontroller uses 5 interfaces (see [here](#)):

- USB interface (to USB connector): connection with the host computer;
- I<sup>2</sup>C interface (to EEPROM): the I<sup>2</sup>C interface connects the USB controller to the EEPROM chip, which stores vendor ID and device ID and the USB firmware. See [chapter DIP Switch](#) for available options.
- SPI interface (to FPGA and Flash): the SPI interface is used to communicate with the FPGA and to access the SPI serial Flash chip. The SPI interface allows a medium-fast (1-2 minutes), frequent and non-volatile configuration (SPI Flash bitstream download) through TE USB FX2 microcontroller and [OpenFutNet](#);
- B2B interface;
- FIFO interface (to FPGA): the FIFO interface provides a high-speed communication channel with the FPGA. The interface can transfer up to 48 MB /s burst rate.



JTAG interface is not directly available to FX2 microcontroller.

## Configuration Mode is selected by mode select pins (M[2:0] or M[1:0]) values

The mode select pins, M[2:0] for Spartan-3E and Spartan-3A (M[1:0] for Spartan-6), define the configuration mode that the FPGA uses to load its bitstream, as shown in Table 2-1. The logic levels applied to the mode pins is sampled on the rising edge of INIT\_B, immediately after the FPGA completes initializing its internal configuration memory. Functional Differences between Spartan-3 Generation Families summarizes the slight differences in functionality between the Spartan-3/6 generation families.

| Spartan 6 FPGA Family |           | Spartan 3 FPGA Family |            |                |
|-----------------------|-----------|-----------------------|------------|----------------|
| M[1:0]                | Spartan-6 | M[2:0]                | Spartan-3E | Spartan-3A DSP |
|                       |           |                       |            |                |

|                   |                                 |         |   |          |
|-------------------|---------------------------------|---------|---|----------|
| <0:1>             | Master Serial/SPI Mode          | <0:0:0> | Master Serial (Platform Flash) Mode (1) |          |
|                   |                                 | <0:0:1> | Master SPI Mode                         |          |
| <0:0>             | Master SelectMAP/BPI (1)        | <0:1:0> | BPI Up (1)                              |          |
|                   |                                 | <0:1:1> | BPI Down (1)                            | Reserved |
| It does not exist |                                 | <1:0:0> | Reserved                                |          |
| <x:x>             | JTAG Mode always available      | <1:0:1> | JTAG Mode, should be selected           |          |
| <1:0>             | Slave Parallel (SelectMAP) Mode | <1:1:0> | Slave Parallel (SelectMAP) Mode         |          |
| <1:1>             | Slave Serial Mode               | <1:1:1> | Slave Serial Mode                       |          |

(1) It is a mode not available in TE USB FX2 modules

#### Mode Pin Settings and Associated FPGA Configuration Mode by Family

- i Among the available modes, Master SPI Mode and JTAG Mode do NOT require support from USB FX2 microcontroller reference firmware; it is only necessary that this two modes do not have interference from this firmware.
- i Among the available modes, Slave Parallel (SelectMAP) Mode and Slave Serial Mode require support from USB FX2 microcontroller firmware; this happens, because it is the only available host (on the TE USB FX2 module) to write configuration data into FPGA and the USB FX2 module could retrieve data from various sources: SPI Flash, USB connection and B2B connection.
- ! USB FX2 microcontroller reference firmware does NOT support Slave Parallel (SelectMAP) Mode and/or Slave Serial Mode; if the user needs to use these configuration modes, he/she should write a custom firmware that load the configuration data from a source (SPI Flash, USB connection or B2B connection) and write the retrieved configuration data in the FPGA.

## Master SPI Mode (TE0300 and TE0320, Bus Width=1) or Master Serial/SPI (TE0630, Bus Width=1,2 or 4)

FPGA configures itself from an attached industry-standard (third-party) SPI serial Flash PROM. The FPGA supplies the CCLK output clock from its internal oscillator and drives the clock input of the attached SPI Flash PROM.

### JTAG Mode

When the FPGA mode pins are set for JTAG mode ( $M[2:0] = <1:0:1>$  in TE0320 and TE0300 module), the FPGA waits to be configured via the JTAG port after a power-on event or after PROG\_B is pulsed Low. Selecting the JTAG mode simply disables the other configuration modes. No other pins are required as part of the configuration interface.

While there is no specific mode for JTAG (in TE0630 module), the JTAG interface is available as a configuration interface any time the device is powered.

### Slave Parallel (SelectMap) Mode

When using Slave Parallel mode configuration, an external host, such as a microprocessor or microcontroller (the USB FX2 microcontroller for the TE USB FX2 module), writes byte-wide configuration data (16 bit are not available in TE USB FX2 modules) into the FPGA, using a typical peripheral interface. See "Slave Parallel (SelectMAP) Mode" of ug332 or "SelectMAP Configuration Interface" of ug380.

### Slave Serial Mode

In Slave Serial mode, an external host such as a microprocessor or microcontroller (the USB FX2 microcontroller for the TE USB FX2 module) writes serial configuration data into the FPGA, using a synchronous serial interface.

## TE0300 module (Spartan-3E): configuration mode available

See also [TE0300 DIP Slide Switch S4 \(Configuration\)](#).

| Spartan-3E (TE0300 module)  |                                  |           |                                | FPGA image (bitstream) could be retrieved from |                                |                               |                   |
|---|----------------------------------|-----------|--------------------------------|--|--------------------------------|-------------------------------|-------------------|
| M[2:0]  | Configuration Mode               | Bus Width | CCLK Direction<br>(FPGA based) | TE0300's SPI<br>Flash<br>memory                | TE0300's<br>Jtag<br>connection | TE0300's<br>USB<br>connection | B2B<br>connection |
| WITHOUT HW modification (desoldering/resoldering) of M10, V11 connection with 3.3V and Gnd, it is only possible to use two type of configurations.    |                                  |           |                                |  |                                |                               |                   |
| <0:0:1>   | Master SPI Mode                  | 1         | Output                         | ✓  | ✗                              | ✗                             | ✗                 |
| <1:0:1>   | JTAG Mode                        | 1         | Input (TCK)                    | ✗  | ✓                              | ✗ <sup>(1)</sup>              | ✓                 |
| WITH HW modification (desoldering/resoldering) of M10, V11 connection with 3.3V and Gnd, it is also possible to use these two type of configurations. |                                  |           |                                |  |                                |                               |                   |
| <1:1:0>   | Slave Parallel (Select MAP) Mode | 8         | Input                          | ✓  | ✗ <sup>(2)</sup>               | ✓                             | ✓                 |
| <1:1:1>   | Slave Serial Mode                | 1         | Input                          | ✓  | ✗ <sup>(2)</sup>               | ✓                             | ✓                 |

### TE0300 Configuration Mode and FPGA image source available

LEGEND:

- ✓ this symbol means that the FPGA image (bitstream) could be retrieved from the source correspondent to the column, using the Configuration Mode correspondent to the row
- ✗ this symbol means that the FPGA image (bitstream) could NOT be retrieved from the source correspondent to the column, using the Configuration Mode correspondent to the row

(1) Do not confuse this connection with the Jtag-USB cable used with TE0300's Jtag connection.

(2) TDI,TDO,TCK and TMS are not connected to USB FX2 microcontroller.

Other 3 configurations are theoretically possible, but these configuration modes require a component not mounted on the TE0300 module.

| <b>M[2:0]</b> | <b>Spartan-3E (TE0300 module)<br/>Configuration Mode</b> | <b>Component required<br/>(not mounted on TE0300 module)</b> |
|---------------|--|--|
| <0:0:0>       | Master Serial (Platform Flash) Mode                      | Xilinx Platform Flash  |
| <0:1:0>       | BPI Up   | third-party BPI Flash  |
| <0:1:1>       | BPI Down   | third-party BPI Flash  |

**Configuration modes unavailable because they require a component not mounted on the TE0300 module.**

TE0320 (Spartan-3A): configuration mode available

See also [TE0320 Mode Select Pins M\[2:0\]](#).

| Spartan-3A DSP (TE0320 module) |                                  |           |                             | Source of FPGA image (bitstream). It could be retrieved from |                          |                         |                |
|--------------------------------|----------------------------------|-----------|-----------------------------|--|--------------------------|-------------------------|----------------|
| M[2:0]                         | Configuration Mode               | Bus Width | CCLK Direction (FPGA based) | TE0320's SPI Flash memory                                    | TE0320's Jtag connection | TE0320's USB connection | B2B connection |
| <0:0:1>                        | Master SPI Mode                  | 1         | Output                      | ✓  | ✗                        | ✗                       | ✗              |
| <1:0:1>                        | JTAG Mode                        | 1         | Input (TCK)                 | ✗  | ✓                        | ✗ <sup>(1)</sup>        | ✓              |
| <1:1:0>                        | Slave Parallel (Select MAP) Mode | 8         | Input                       | ✓  | ✗ <sup>(2)</sup>         | ✓                       | ✓              |
| <1:1:1>                        | Slave Serial Mode                | 1         | Input                       | ✓  | ✗ <sup>(2)</sup>         | ✓                       | ✓              |

**TE0320 Configuration Mode and FPGA image source available**

LEGEND:

- ✓ this symbol means that the FPGA image (bitstream) could be retrieved from the source correspondent to the column, using the Configuration Mode correspondent to the row
- ✗ this symbol means that the FPGA image (bitstream) could NOT be retrieved from the source correspondent to the column, using the Configuration Mode correspondent to the row

(1) Do not confuse this connection with the Jtag-USB cable used with TE0320's Jtag connection.

(2) TDI,TDO,TCK and TMS are not connected to USB FX2 microcontroller.

Other 2 configurations are theoretically possible, but these configurations require a component not mounted on the TE0320 module.



| M[2:0]  | Spartan-3A DSP (TE0320 module)<br>Configuration Mode | Component required<br>(not mounted on TE0320 module) |
|---------|--|--|
| <0:0:0> | Master Serial (Platform Flash) Mode                  | Xilinx Platform Flash                                |
| <0:1:0> | BPI Up   | third-party BPI Flash                                |

Configuration modes unavailable because they require a component not mounted on the TE0320 module

## TE0630 (Spartan-6): configuration mode available

All mode selection pins are hardwired (they do not exist as switches).

| Spartan-6 (TE0630 module)  |                                 |                  |                                | Source of FPGA image (bitstream). It could be retrieved from |                                |                               |                               |
|--|---------------------------------|------------------|--------------------------------|--|--------------------------------|-------------------------------|-------------------------------|
| M[1:0]   | Configuration Mode              | Bus Width        | CCLK Direction<br>(FPGA based) | TE0630's SPI Flash<br>memory                                 | TE0630's<br>Jtag<br>connection | TE0630's<br>USB<br>connection | TE0630's<br>B2B<br>connection |
| WITHOUT HW modification (desoldering/resoldering) of U15, Y18 connection with 3.3V and Gnd, it is only possible to use two type of configurations. |                                 |                  |                                |  |                                |                               |                               |
| <0:1>  | Master Serial/SPI               | 1,2 or 4         | Output                         | ✓  | ✗                              | ✗                             | ✗                             |
| <x:x> <sup>(1)</sup>   | JTAG Mode                       | 1                | Input (TCK)                    | ✗  | ✓                              | ✗ <sup>(2)</sup>              | ✓                             |
| WITH HW modification (desoldering/resoldering) of U15, Y18 connection with 3.3V and Gnd, it is only possible to use two type of configurations.    |                                 |                  |                                |  |                                |                               |                               |
| <1:0>  | Slave Parallel (SelectMap) Mode | 8 <sup>(3)</sup> | Input                          | ✓  | ✗ <sup>(4)</sup>               | ✓                             | ✓                             |
| <1:1>  | Slave Serial Mode               | 1                | Input                          | ✓  | ✗ <sup>(4)</sup>               | ✓                             | ✓                             |

### TE0630 Configuration Mode and FPGA image source available

LEGEND:

- ✓ this symbol means that the FPGA image (bitstream) could be retrieved from the source correspondent to the column, using the Configuration Mode correspondent to the row
- ✗ this symbol means that the FPGA image (bitstream) could NOT be retrieved from the source correspondent to the column, using the Configuration Mode correspondent to the row

(1) Spartan-6 devices also have a dedicated four-wire JTAG (IEEE Std 1149.1) port that is always available to the FPGA regardless of the mode pin settings.

(2) Do not confuse this connection with the Jtag-USB cable used with TE0630's Jtag connection.

(3) 16 bit interface is theoretically possible but is not supported in the TE0630 module.

(4) TDI,TDO,TCK and TMS are not connected to USB FX2 microcontroller.

Another configuration is theoretically possible, but this configuration requires a component not mounted on the TE0630 module.

| M[1:0] | Spartan-6 (TE0630 module)<br>Configuration Mode | Component required<br>(not mounted on TE0630 module) |
|--------|---|--|
| <0:0>  | Master SelectMAP/BPI                            | third-party BPI Flash                                |

**Configuration modes unavailable because they require a component not mounted on the TE0630 module**