TE0320 Assembly Options Overview

module	FPGA device	power supply source	VcccIO0	mnemonics
TE0320-00-EV01	XC3SD1800A-4FGG676C	USB	3.3 V	evaluation
TE0320-00-EV02	XC3SD1800A-4FGG676C	B2B	3.3 V	evaluation
TE0320-00-EV02B	XC3SD3400A-4FGG676C	B2B	3.3 V	evaluation, big

Assembly options overview.

To determine the FPGA device, you just read the code on the package under the "Xilinx Spartan" label.
To determine the power supply source, please see ~~paragraph 5.2~~ Power Supply Sources.
To determine the VcccIO0 voltage, please see ~~paragraph 5.3~~ On-Board Power Rails.
To determine PCB revision and assembly variant from FPGA, TE0320 have dedicated user signals, which can be read by user core.
Board revision coded in 4 bits REV[3:0]

Signal name	FPGA pin
REV0	C21
REV1	D21
REV2	E21
REV3	C20

Board revision pins

To define low (zero) level REV pin connected to ground rail, to define high (one) level REV pin left float (open). These pins should be configured with "pullup" option in user design.
See the table below for current list of board revisions.

REV3	REV2	REV1	REV0	Board revision
1	1	1	1	Revision 00

Board revisions

Module assembly variant encoded using VAR[5:0] pins.

Signal name	FPGA pin
VAR0	F17
VAR1	K16
VAR2	J16
VAR3	E17
VAR4	D20
VAR5	A20

Assembly variants pins

To define low (zero) level VAR pin connected to ground rail through zero resistor, to define high (one) level VAR pin left float (open). These pins should be configured with "pullup" option in user design.
Available module assembly variants listed in the table below.

VAR5	VAR4	VAR3	VAR2	VAR1	VAR0	Variant
1	1	1	1	1	1	EV01
1	1	1	1	1	0	EV02

Module assembly variants