TE0320 Clock Network

24 MHz Clock Oscillator

The module has a 24 MHz SMD clock oscillator providing a clock source for both the EZ-USB FX2LP USB FX2 microcontroller (XTALIN) and the FPGA as detailed in the table below.

signal	FPGA pin	FPGA ball	FPGA bank
24MHZ1	IO_L28N_2 GCLK3	AE14	2

24 MHz clock signal details.

Digital Clock Manager (DCM)

The DCMs of the FPGA can be used to synthesize arbitrary clock frequencies from any on-board clock network, differential clock input pair or single-ended clock input. For further reference, please read Xilinx DS485:Digital Clock Manager (DCM) Module and the DCM chapter in Xilinx UG331: Spartan-3 Generation FPGA User Guide.

Interface Clock (IFCLK)

The IFCLK line synchronizes the communication between the EZ-USB FX2LP USB FX2 microcontroller and the FPGA as detailed in the table below.

signal	FPGA pin	FPGA ball	FPGA bank
IFCLK	IO_L31N_1 TRDY1 RHCLK3	P25	1

Interface clock (IFCLK) signal details.

Main Clock Oscillator

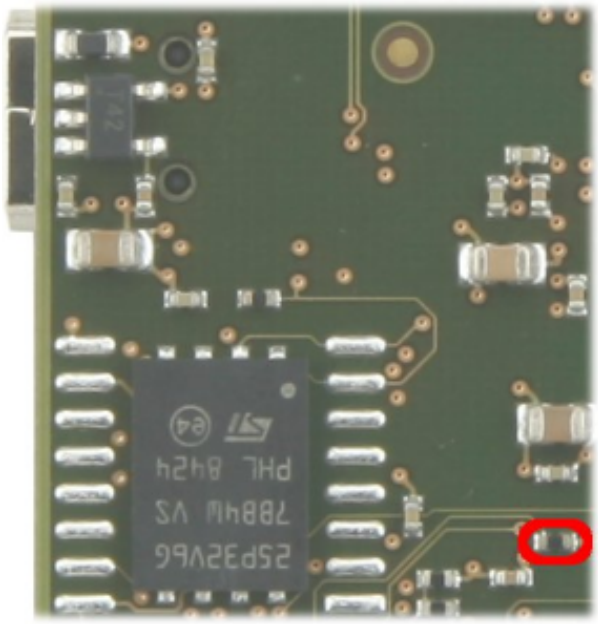
The module has a main SMD clock oscillator providing a clock source for the FPGA as detailed in the table below.

signal	FPGA pin	FPGA ball	FPGA bank
MAINCLK	IO_L27N_2 GCLK1	AA14	2

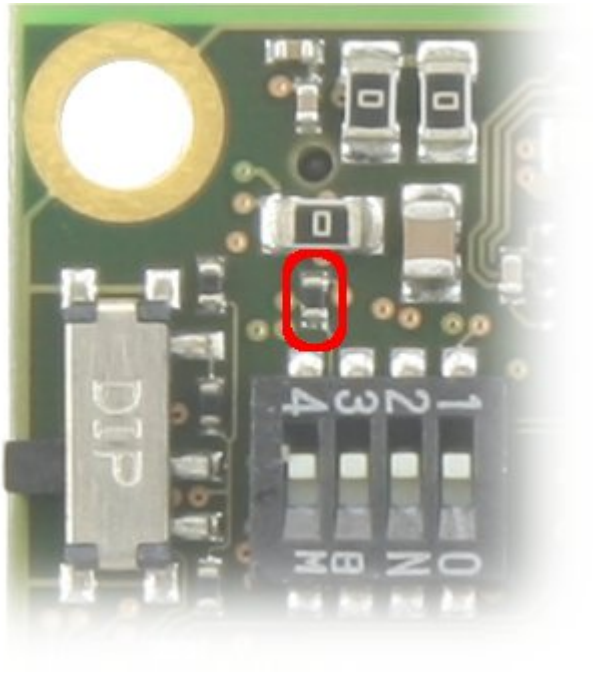
Main clock signal details.
Standard frequency is 100 MHz. Should you wish or need another main clock oscillator frequency, please contact Trenz Electronic. The lower the main clock frequency, the lower the module power consumption. Moreover, as the main clock is preferably used as DDR SDRAM clock, a lower clock frequency makes easier for the development tools to meet the timing requirements (particularly for DDR SDRAM).

Watchdog Timer

TE0320 has a watchdog timer that is periodically triggered by a positive or negative transition of the watchdog input (WDI) signal. When the supervising system fails to retrigger the watchdog circuit within the time-out interval (min 1.1 s, typ 1.6 s, max 2.3 s), the watchdog output becomes active and asserts the master reset (/MR) signal. This event also reinitializes the watchdog timer.
If resistors R135 and R136 are not populated, the watchdog is disabled.
If resistors R135 and R136 are populated, the watchdog can be enabled (or not).



R135 (bottom side).



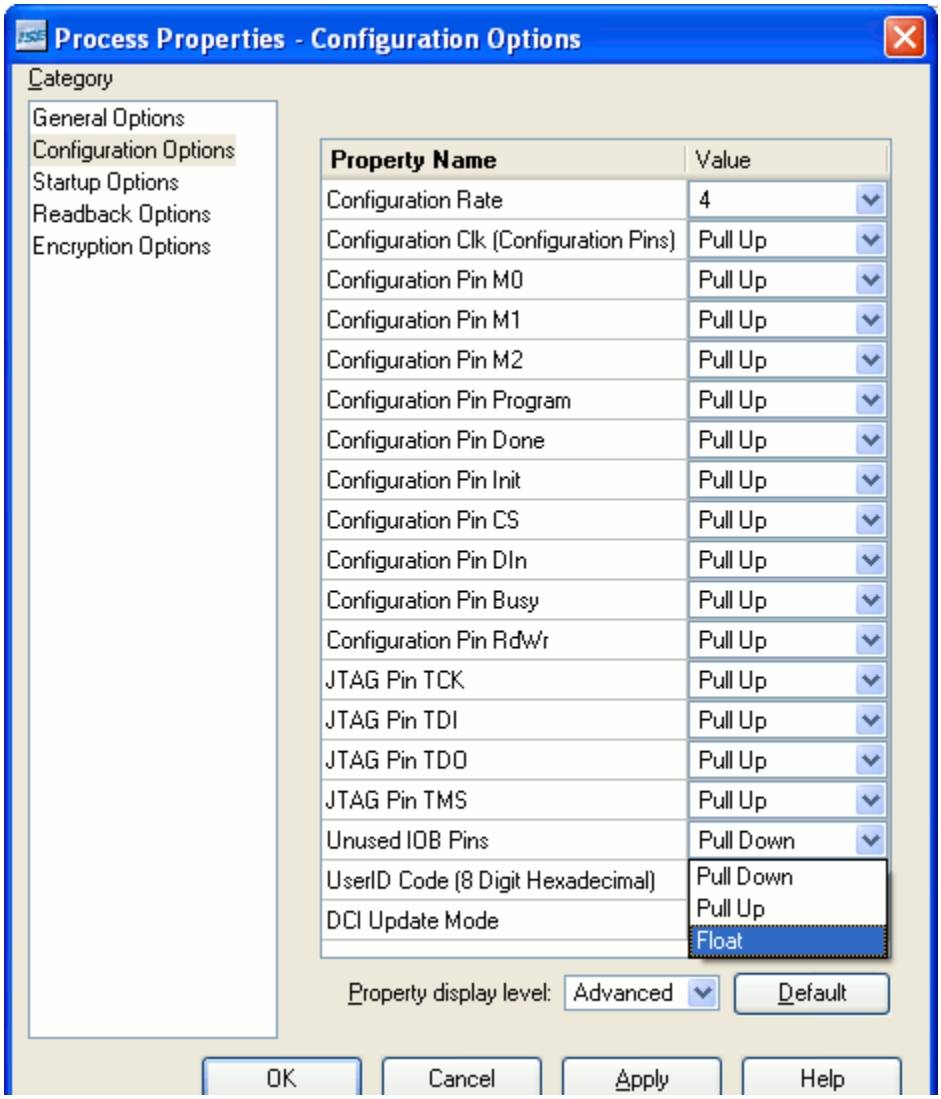
R136 (top side).

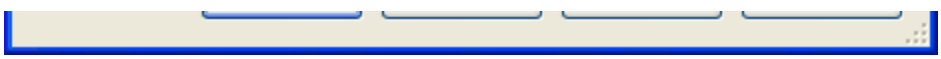
R135, R136 Watchdog

> Any other combination of resistors R135 and R136 is not supported.

If resistors R135 and R136 are populated, there is two configuration possible.

- To enable the watchdog after module power-up, drive the WDI signal to generate a transition (no matter if positive or negative).
- To keep the watchdog disabled, set the WDI FPGA signal output to high-impedance. One way to reach this goal is to leave FPGA pin V24 (FPGA signal IO_L19P_1) undeclared in the user constraints file (UCF) and set the Xilinx Project Navigator options as follows: project properties > configuration options > unused IOB pins > float.


Process Properties - Configuration Options
Category
General Options
Configuration Options
Startup Options
Readback Options
Encryption Options
Property Name
Value
Configuration Rate
4
Configuration Clk (Configuration Pins)
Pull Up
Configuration Pin M0
Pull Up
Configuration Pin M1
Pull Up
Configuration Pin M2
Pull Up
Configuration Pin Program
Pull Up
Configuration Pin Done
Pull Up
Configuration Pin Init
Pull Up
Configuration Pin CS
Pull Up
Configuration Pin DIn
Pull Up
Configuration Pin Busy
Pull Up
Configuration Pin RdWr
Pull Up
JTAG Pin TCK
Pull Up
JTAG Pin TDI
Pull Up
JTAG Pin TDO
Pull Up
JTAG Pin TMS
Pull Up
Unused IOB Pins
Pull Down
UserID Code (8 Digit Hexadecimal)
DCI Update Mode
Pull Down
Pull Up
Float
Property display level:
Advanced
Default
OK
Cancel
Apply
Help



Configuration option in Xilinx ISE Project Navigator.