TE0320 FPGA Configuration Using SPI Indirect In-System Programming (ISP)

DIP Switches Configuration

Similar to the traditional configuration memories, SPI serial Flash memories must be loaded with the configuration data. SPI serial Flash memories have a single interface for programming, but there are multiple methods to deliver the data to this interface. This section discusses the hardware setup, the PROM file generation flow and the software flow for ISP (indirect in-system programming) of a Trenz Electronic TE0320 SPI serial Flash configuration PROM through the JTAG interface of a Xilinx Spartan-3A DSP FPGA using Xilinx iMPACT 11.5 (with other version the procedure should be almost the same).
To write the SPI Flash memory, perform the following steps:

1. disable the master reset S1D (do not care about all other switches at write time);
2. connect the Xilinx platform cable to JTAG connector J2;
3. generate or locate the FPGA bitstream file you want to store on the memory;
4. prepare an SPI PROM file using the ISE iMPACT graphical software from the FPGA bitstream file (link);
5. use the ISE iMPACT graphical software to in-system program the SPI PROM (link).

In order to have the module to configure from its SPI Flash memory next time it is (re)booted, ensure one of following DIP switch settings:

switch	S1A (EEPROM serial data)	S1B (M2)	S1C (M1)	S1D (/MR master reset)	S2 (PS_EN)
state	0 = ON	0 = ON	0 = ON	1 = OFF	X = do note care
state	1 = OFF	0 = ON	0 = ON	1 = OFF	FX2 PON

S1 settings for booting from SPI Flash memory.