Porting to different modules

Example of porting to a different module

The supplied reference designs were built for typical TE0300, TE0320 and TE0630. Normally, you don't need to port the reference design.

If the module used are slightly different from typical, you can use the following example as a guide to port the design to your board.

The supplied reference design of the example were built for typical TE0300-01 which uses a 125MHz oscillator and a Spartan-3E XC3S1200E-4FG320 FPGA. Other module assembly versions are listed in the table below.

moduleversion	kilo gates	env.	clock [MHZ]	memory (DDR SDRAM)
TE0300-01	1200	Com	125	Qimonda HYB25DC512160CF-6
TE0300-01M	1200	Com	125	Micron MT46V32M16BN-6:F
TE0300-01B	1600	Com	125	Qimonda HYB25DC512160CF-6
TE0300-01BM	1600	Com	125	Micron MT46V32M16BN-6:F
TE0300-01BLP	1600	Com	100	Qimonda HYB25DC512160CF-6
TE0300-01BMLP	1600	Com	100	Micron MT46V32M16BN-6:F
TE0300-01I	1200	Ind	125	Micron MT46V32M16BN-6 IT:F
TE0300-01IBM	1600	Ind	125	Micron MT46V32M16BN-6 IT:F

TE0300 assembly versions.

- "Com" is "commercial grade" and "Ind" is "industrial grade";
- 100 or 125 MHz are oscillator frequencies;
- MT46V32M16BN-6 IT:F is a Micron Technologies industrial DDR SDRAM memory, while the others are commercial ones.

To change the FPGA device, you should

- open the project in Xilinx Platform Studio;
- click on the "Project" tab;
- under "Project Options" double click on "Device";
- select a suitable FPGA device.

The example shows the case of a Spartan-3E xc3s1200e (or xc3s1600e)/fg320/-4.

The DDR constraints are different for different device sizes. Otherwise you get timing / routing errors.
To change oscillator frequency, we advice you to manually edit *system.mhs*. You can open it by double clicking on "MHS File" under "Project Files":
Edit the input clock freq in Hz (100000000 or 125000000):
PORT sys_clk_pin = dcm_clk_s, DIR = I, SIGIS = DCMCLK, CLK_FREQ =125000000
Adjust clock generator frequencies by replacing all "125" occurrences by 100 and all "500" occurrences by 625 or the other way around:
BEGIN clock_generator
PARAMETER INSTANCE = clock_generator_0
PARAMETER HW_VER = 2.01.a
PARAMETER C_EXT_RESET_HIGH = 1
PARAMETER C_CLKIN_FREQ =125000000
PARAMETER C_CLKOUT0_FREQ =62500000
PARAMETER C_CLKOUT0_PHASE = 0
PARAMETER C_CLKOUT0_GROUP = NONE
PARAMETER C_CLKOUT1_FREQ =125000000
PARAMETER C_CLKOUT1_PHASE = 0
PARAMETER C_CLKOUT1_GROUP = NONE
PARAMETER C_CLKOUT2_FREQ =125000000
PARAMETER C_CLKOUT2_PHASE = 90
PARAMETER C_CLKOUT2_GROUP = NONE
PARAMETER C_CLKIN_BUF = FALSE
PARAMETER C_CLKOUT0_BUF = TRUE
PARAMETER C_CLKOUT1_BUF = TRUE
PARAMETER C_CLKOUT2_BUF = TRUE
PORT CLKOUT0 = sys_clk_s
PORT CLKOUT1 = DDR_SDRAM_mpmc_clk_s
PORT CLKOUT2 = DDR_SDRAM_mpmc_clk_90_s
PORT CLKIN = dcm_clk_s
PORT LOCKED = clock_generator_locked
PORT RST = net_gnd
END

Adjust memory controller parameters to appropriate values:
BEGIN mpmc
PARAMETER INSTANCE = DDR_SDRAM
PARAMETER HW_VER = 4.03.a
PARAMETER C_NUM_PORTS = 3
PARAMETER C_PIM0_BASETYPE = 1
PARAMETER C_PIM1_BASETYPE = 1
PARAMETER C_MEM_PARTNO =HYB25D512160BF-6 (or MT46V32M16-6)
PARAMETER C_MEM_DATA_WIDTH = 16
PARAMETER C_MEM_TYPE = DDR
PARAMETER C_XCL0_WRITEXFER = 0
PARAMETER C_PIM2_BASETYPE = 6
PARAMETER C_MPMC_CLK0_PERIOD_PS =8000 (or 10000)
PARAMETER C_MPMC_BASEADDR = 0x1C000000
PARAMETER C_MPMC_HIGHADDR = 0x1FFFFFFF
PARAMETER C_PIM2_DATA_WIDTH = 32
Adjust also UARTLITE system clock frequency (if you need UART on external pins of course):
BEGIN xps_uartlite
PARAMETER INSTANCE = RS232
PARAMETER HW_VER = 1.00.a
PARAMETER C_SPLB_CLK_FREQ_HZ =62500000
PARAMETER C_BAUDRATE = 115200
PARAMETER C_ODD_PARITY = 0
PARAMETER C_USE_PARITY = 0
PARAMETER C_BASEADDR = 0x84000000
PARAMETER C_HIGHADDR = 0x8400ffff
BUS_INTERFACE SPLB = mb_plb
PORT RX = fpga_0_RS232_RX
PORT TX = fpga_0_RS232_TX
PORT Interrupt = RS232_Interrupt
END

That is all.

Then download the bitstream file to the FPGA.