Recomended Design Tools Settings

Common to all USB FX2 Modules

Unused IOB Pin

All signals entering and exiting a Xilinx Spartan-3 and Spartan-6 generation FPGA must pass through the I/O resources, known as I/O blocks or IOBs. Users can specify the configuration for any unused IOB pins. This is the serial data outputs for all JTAG instruction and data registers.

This options are set graphically in Xilinx ISE Software Project Navigator by selecting the following:
Generate Programming File > Process Properties > Configuration Options > Unused IOB Pins
Select an option from the drop-down list.

1. Pull DownDefault. All unused I/O pins and input-only pins have a pull-down resistor to GND.
2. Pull UpAll unused I/O pins and input-only pins have a pull-up resistor to the VCCO_# supply for its associated I/O bank.
3. Float (also: Pullnone)All unused I/O pins and input-only pins are left floating (Hi-Z, high-impedance, three-state). Use external pull-up or pulldown resistors or logic to apply a valid signal level.

CCLK Frequency

In SPI Flash mode, the FPGA's internal oscillator generates the configuration clock frequency. The FPGA provides this clock on its CCLK output pin, driving the PROM's Slave Clock input pin. The FPGA begins configuring using its lowest frequency setting. If so specified in the configuration bitstream, the FPGA increases the CCLK frequency to the specified setting for the remainder of the configuration process. The maximum frequency is specified using the ConfigRate bitstream generator option. The maximum frequency supported by the FPGA configuration logic depends on the timing for the SPI Flash device. For TE0300, TE0320 and TE0630 SPI Flash PROM use ConfigRate = 12 or lower.

This options are set graphically in Xilinx ISE Software Project Navigator by selecting the following:

- Generate Programming File > Process Properties > Configuration Options > Configuration Rate > 12 (or lower)

Not common to all USB FX2 Modules

TE0300

WattchDog: no.

EEPROM connection disabled: S1 = OFF

EEPROM connection enabled: S1 = ON

See switches for more information.

TE0320

WatchDog : yes.

EEPROM connection disabled: S1A = OFF

EEPROM connection enabled: S1A = ON

See switches for more information.

TE0630

WattchDog: no.

EEPROM connection disabled: S1A = OFF

EEPROM connection enabled: S1A = ON

See switches for more information.