Configuration of USB (firmware, EEPROM) and FPGA (bitstream, SPI Flash)

USB FX2 microcontroller Configuration (RAM Firmware)

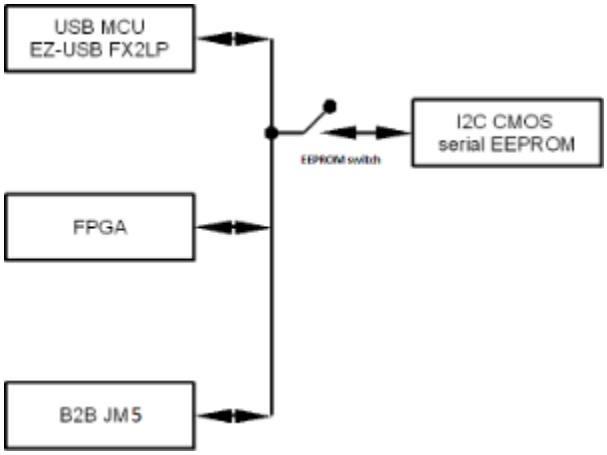
You can use CyConsole ("Options" > "EZ-USB Interface" > "Download" and a .hex or .bix file) or CyControl ("Program FX2 > RAM" and a .hex or .iic file) to directly program the firmware file (.hex, .bix or .iic file) into the USB FX2 microcontroller's RAM.

You can also use OpenFutNet: if used for Firwmare Recovery Boot or Firmware Upgade both EEPROM and RAM are programmed.

If you don't also write the IIC EEPROM ("Options" > "EZ-USB Interface" > "Lg EEPROM" for CyConsole and "Program>FX2 64KB EEPROM" for CyControl), the new firmware is lost if the TE USB FX2 module goes under reset or power off/on cycle.

IIC EEPROM Configuration (EEPROM Firmware)

If the TE USB FX2 module exit from reset or is powered on, the IIC EEPROM content programs/configures the USB FX2 microcontroller RAM



IIC EEPROM and USB FX2 microcontroller connection.

You can use CyConsole ("Lg EEPROM") and CyControl ("Program>FX2 64KB EEPROM") to directly program the .iic Firmware file into the IIC EEPROM connected to USB FX2 microcontroller.

You can also use OpenFutNet: if used for Firwmare Recovery Boot or Firmware Upgade both EEPROM and RAM are programmed.

The firmware actually changes (it runs on USB FX2 microcontroller's RAM) only when

- you reset the TE USB FX2 module;
- you power off and power on the TE USB FX2 module;
- you write the USB FX2 microcontroller's RAM (but the new firmware is lost if the TE USB FX2 module goes under reset or power off/on cycle).

FPGA Configuration (bitstream, RAM-like image)

If you don't also write the SPI Flash memory, the new bitstream image is lost if the TE USB FX2 module goes under reset or power off/on cycle.

The Xilinx Spartan-3E FPGA on the TE0300, Xilinx Spartan-3A DSP FPGA on the TE0320, Xilinx Spartan-6 FPGA on the TE0630 can be configured in the following ways:

- B2B connector
  - JTAG
  - Slave Parallel (SelectMAP)
  - Slave Parallel
- 6-pin JTAG header connector
- 6-pin SPI header connector (TE0300 only)
- USB connector (in fact, SPI Flash memory is used: OpenFutNet or another softwares writes the bitstream image in the SPI Flash and, after SPI Flash writing is complete, the FPGA read the SPI Flash content to configure itself)
- SPI Flash memory (see the next section)

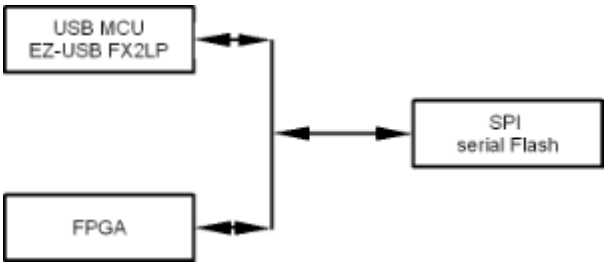
Programming using JTAG interface provide convenient and fast way to test FPGA project. FPGA configuration programmed this way is volatile and lost after reset or power cycle.

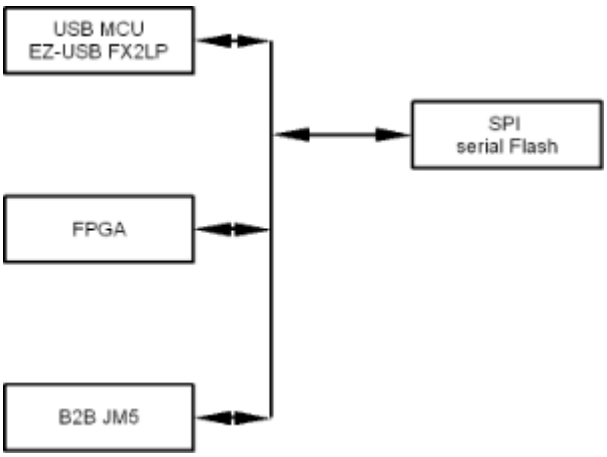
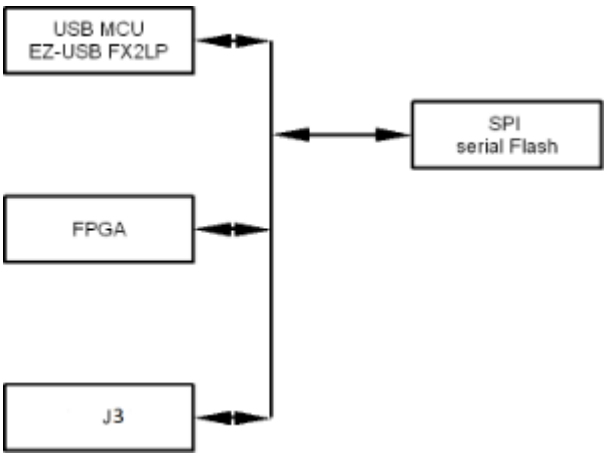
For further information on

- Xilinx Spartan-3E FPGA
- Xilinx Spartan-3A DSP configuration modes, please consult the documentation listed in chapter 17 Related Materials and References.
- Xilinx Spartan-6

SPI Flash Configuration (bitstream, PROM image)

If the TE USB FX2 module exit from reset state or is powered on (in the default state of switches), the SPI Flash content programs/configures the FPGA.

TE USB FX2 module type	SPI Bus connection
TE0630	

TE0320	
TE0300	

SPI Flash and FPGA connection; SPI Flash and USB FX2 microcontroller

The bit-stream for the FPGA is stored in the SPI Flash. To use this bit-stream source FPGA configuration option is set to “Master Serial/SPI”. See SPI Flash Bus links for additional information for every case.

SPI Flash can be programmed in several ways:

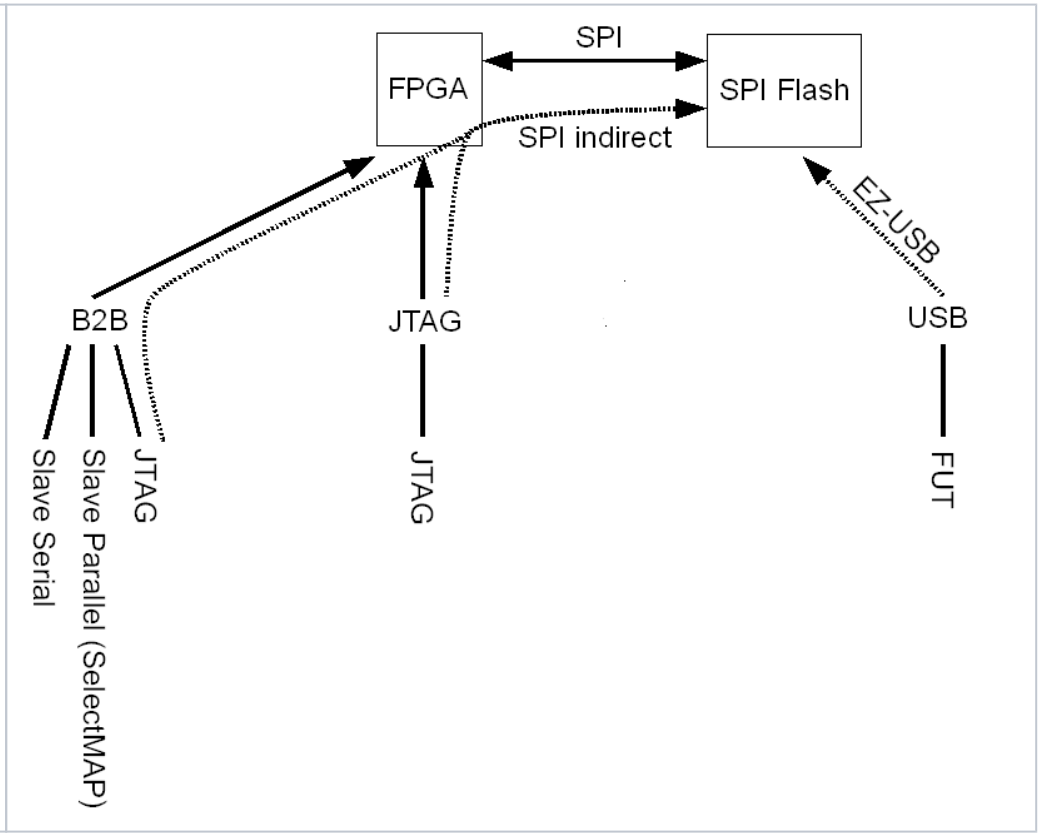
- Direct programming via USB controller; it is usually done by Firmware Upgrade Tools like Python OpenFut and C# OpenFutNet.
- Indirect SPI programming via FPGA pins; it is done by Xilinx iMPACT via JTAG. See Appendix A. Indirect SPI Programming using iMPACT.
- Direct SPI programming via FPGA pins; the FPGA project should contain SPI interface core and the software to work with it (SPI interface and SW required are automatically created by Xilinx iMPACT tool). Only if Xilinx iMPACT tool is version 11.x or below, see Xilinx AR#36156.

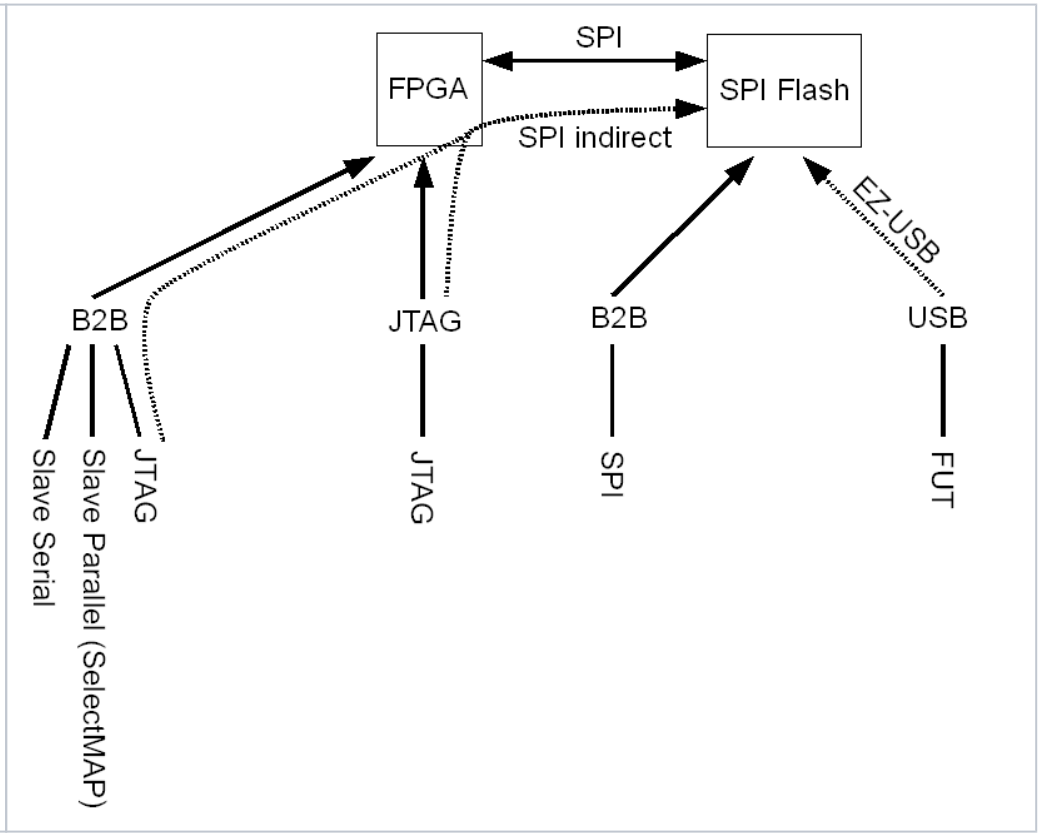
SPI Flash can be programmed using the following connection:

- USB connector
- B2B connector
  - JTAG
  - Slave Parallel (SelectMAP)
  - Slave Serial
- 6-pin JTAG header connector
- 6-pin SPI header connector (TE0300 only)

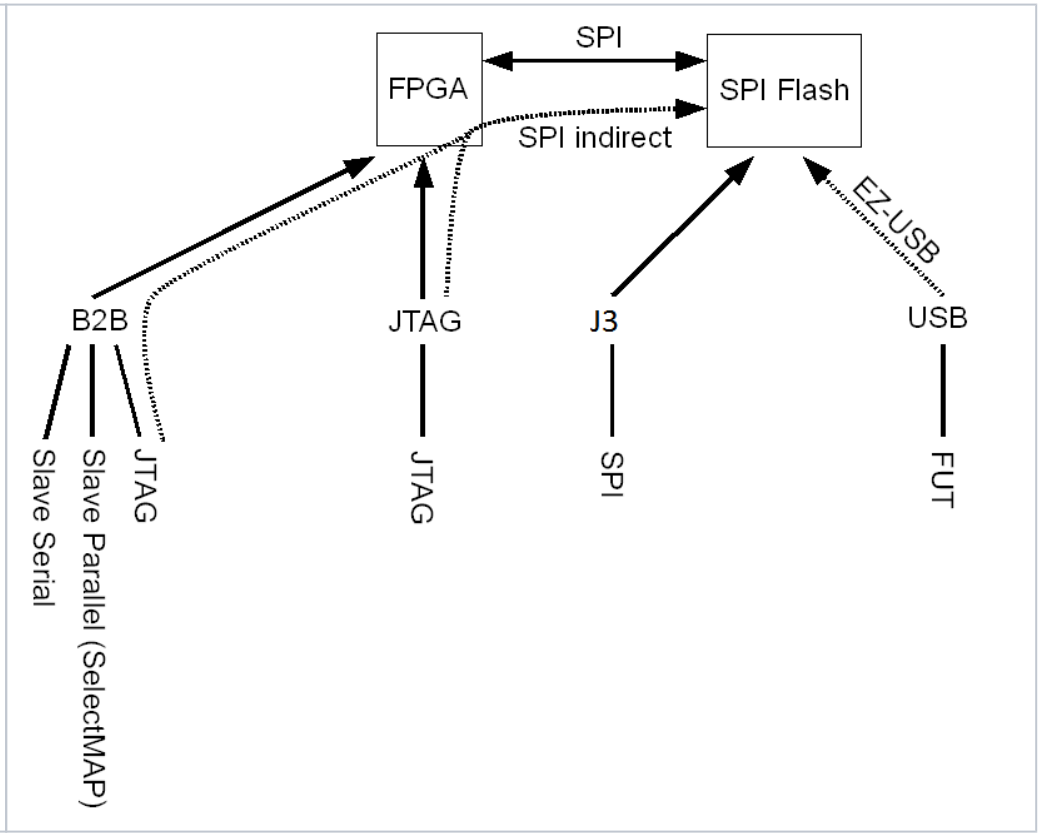
TE USB FX2 module type	Configuration mode connection

TE0630


SPI
FPGA
SPI Flash
SPI indirect
EZ-USB
B2B
JTAG
USB
Slave Serial
Slave Parallel (SelectMAP)
JTAG
JTAG
FUT

TE0320	 SPI FPGA SPI Flash SPI indirect EZ-USB B2B JTAG B2B USB Slave Serial Slave Parallel (SelectMAP) JTAG JTAG SPI FUT

TE0300



Configuration modes overview.