TE0320 B2B Connectors Pin Descriptions

This section describes how the various pins on B2B connectors JM4 and JM5 connect with TE0320 on-board components. In this chapter, most of naming conventions and colour coding scheme are taken from the official Xilinx Spartan-3A DSP documentation.

> The connection between TE0320 module connectors JM4/JM5 and TE0323 Prototyping Carrier Board connectors J1/J2/J3/J4 is documented here.

Pin Labelling

The pin label is abbreviated but descriptive for each pin. All I/O pins begin with IO. If a pin can be used as a differential signal, the name includes an _Lxxy_b suffix, where

- L indicates that the pin is part of a differential pair
- xx is a two-digit integer, unique for each bank, that identifies a differential pin-pair
- y is the signal polarity and is replaced by P for the positive signal or N for the negative. These two pins form one differential pin-pair
- b is an integer, 0 through 2 for TE0320, indicating the associated I/O bank.

Dual- or multi-purpose pins have a name composed of the signal names referring to each possible pin function (e. g. IO_L52P_2 / D0 / DIN / MISO). _B is used as the active-Low designator, as in CSI_B.

A differential clock input requires two global clock inputs. The P and N inputs follow the same configuration as for standard inputs on those pins. The clock inputs that get paired together are consecutive pins in clock number, an even clock number and the next higher odd value. For example, GCLK0 and GCLK1 are a differential pair.

Pin Types

Most pins of B2B connectors JM4 and JM5 are general-purpose, user-defined I/O pins (GPIOs). There are, however, up to 9 different functional types of pins on the TE0320, as outlined in the table below. In pin-out tables JM4 and JM5, the individual pins are colour-coded according to pin type as in the table below.

type color code	type of pins description
I/O	Unrestricted, general-purpose user-I/O pin. Most pins can be paired together to form differential I/Os.
DUAL	Dual-purpose pin used in some configuration modes during the configuration process and then usually available as a user I/O after configuration. If the pin is not used during configuration, this pin behaves as an I/O-type pin. See Xilinx UG332: Spartan-3 Generation Configuration User Guide for additional information on these signals.
VREF	VREF0 provides a reference voltage input for certain I/O standards. See Voltage Reference VREF0 for additional information on this signal.
CLK	Either a user-I/O pin or an input to a specific clock buffer driver. Packages have 16 global clock inputs that optionally clock the entire device. See the Using Global Clock Resources chapter in UG331: Spartan-3 Generation FPGA User Guide for additional information on these signals.
CONFIG	Dedicated configuration pin, two per device. Not available as a user-I/O pin. Every package has two dedicated configuration pins. These pins are powered by VCCAUX. See Xilinx UG332: Spartan-3 Generation Configuration User Guide for additional information on these signals.
PWRMGMT	Control and status pins for the power-saving Suspend mode. SUSPEND is a dedicated pin and is powered by VCCAUX. AWAKE is a Dual-Purpose pin. Unless Suspend mode is enabled in the application, AWAKE is available as a user-I/O pin.
JTAG	Dedicated JTAG pin - 4 per device. Not available as a user-I/O pin. Every package has four dedicated JTAG pins. These pins are powered by VCCAUX.
GND	Dedicated ground pin. All must be connected.
TE	Trenz Electronic specific pin type. See the description of each pin in the user manual for additional information on the corresponding signals.

Types of pins on TE0320

B2B Connector Pin-Outs

Connector JM4: Pin-Out information

supply	bank	type	FPGA pin	FPGA ball	JM4 signal	JM4 pin	JM4 pin	JM4 singal	FPGA ball	FPGA pin	type	bank	supply
3.3 V	-	out	-	-	3.3V	1	2	GND	-	-	GND	GND	GND
VcccIO0	0	I/O	IO_L20P_0	F15	JM4-IO01	3	4	B2B_D_P	-	-	I/O	-	USB
VcccIO0	0	I/O	IO_L21N_0	C16	JM4-IO02	5	6	B2B_D_N	-	-	I/O	-	USB
GND	GND	GND	-	-	GND	7	8	JM4-IO34	K12	IO_L39N_0	I/O	0	VcccIO0
VcccIO0	0	I/O	IO_L21P_0	D17	JM4-IO03	9	10	JM4-IO35	J12	IO_L39P_0	I/O	0	VcccIO0
VcccIO0	0	I/O	IO_L22N_0	C15	JM4-IO04	11	12	JM4-IO36	D8	IO_L40N_0	I/O	0	VcccIO0
VcccIO0	0	I/O	IO_L22P_0	D16	JM4-IO05	13	14	JM4-IO37	C8	IO_L40P_0	I/O	0	VcccIO0
VcccIO0	0	I/O	IO_L23N_0	A15	JM4-IO06	15	16	GND	-	-	GND	GND	GND
VcccIO0	0	I/O	IO_L23P_0	B15	JM4-IO07	17	18	JM4-IO38	C6	IO_L41N_0	I/O	0	VcccIO0
VcccIO0	0	I/O	IO_L24N_0	F14	JM4-IO08	19	20	JM4-IO39	B6	IO_L41P_0	I/O	0	VcccIO0
VcccIO0	0	I/O	IO_L24P_0	E14	JM4-IO09	21	22	JM4-IO40	C7	IO_L42N_0	I/O	0	VcccIO0
GND	GND	GND	-	-	GND	23	24	JM4-IO41	B7	IO_L42P_0	I/O	0	VcccIO0
VcccIO0	0	I/O GCLK	IO_L25N_0 GCLK5	J14	JM4-IO10	25	26	JM4-IO42	K11	IO_L43N_0	I/O	0	VcccIO0
VcccIO0	0	I/O GCLK	IO_L25P_0 GCLK4	K14	JM4-IO11	27	28	JM4-IO43	J11	IO_L43P_0	I/O	0	VcccIO0
VcccIO0	0	I/O GCLK	IO_L26N_0 GCLK7	A14	JM4-IO12	29	30	VcccIO0	-	-	I/O	0	VcccIO0
VcccIO0	0	I/O GCLK	IO_L26P_0 GCLK6	B14	JM4-IO13	31	32	JM4-IO44	D6	IO_L44N_0	I/O	0	VcccIO0
VcccIO0	0	I/O GCLK	IO_L27N_0 GCLK9	G13	JM4-IO14	33	34	JM4-IO45	C5	IO_L44P_0	I/O	0	VcccIO0
VcccIO0	0	I/O GCLK	IO_L27P_0 GCLK8	F13	JM4-IO15	35	36	JM4-IO46	B4	IO_L45N_0	I/O	0	VcccIO0
VREF	0	in	-	-	VREF0	37	38	JM4-IO47	A4	IO_L45P_0	I/O	0	VcccIO0
VcccIO0	0	I/O GCLK	IO_L28N_0 GCLK11	C13	JM4-IO16	39	40	JM4-IO48	H10	IO_L46N_0	I/O	0	VcccIO0
VcccIO0	0	I/O GCLK	IO_L28P_0 GCLK10	B13	JM4-IO17	41	42	JM4-IO49	G10	IO_L46P_0	I/O	0	VcccIO0
VcccIO0	0	I/O	IO_L29N_0	B12	JM4-IO18	43	44	VcccIO0	-	-	I/O	0	VcccIO0
VcccIO0	0	I/O	IO_L29P_0	A12	JM4-IO19	45	46	JM4-IO50	H9	IO_L47N_0	I/O	0	VcccIO0
VcccIO0	0	I/O	IO_L30N_0	C12	JM4-IO20	47	48	JM4-IO51	G9	IO_L47P_0	I/O	0	VcccIO0
VcccIO0	0	I/O	IO_L30P_0	D13	JM4-IO21	49	50	JM4-IO52	E7	IO_L48N_0	I/O	0	VcccIO0
GND	GND	GND	-	-	GND	51	52	JM4-IO53	F7	IO_L48P_0	I/O	0	VcccIO0
VcccIO0	0	I/O	IO_L33N_0	B10	JM4-IO22	53	54	JM4-IO54	B3	IO_L51N_0	I/O	0	VcccIO0
VcccIO0	0	I/O	IO_L33P_0	A10	JM4-IO23	55	56	JM4-IO55	A3	IO_L51P_0	I/O	0	VcccIO0
VcccIO0	0	I/O	IO_L34N_0	D10	JM4-IO24	57	58	GND	-	-	GND	GND	GND
VcccIO0	0	I/O	IO_L34P_0	C10	JM4-IO25	59	60	JM4-IO56	C23	IO_L06N_0	I/O	0	VcccIO0
VcccIO0	0	I/O	IO_L35N_0	H12	JM4-IO26	61	62	JM4-IO57	D23	IO_L06P_0	I/O	0	VcccIO0
VcccIO0	0	I/O	IO_L35P_0	G12	JM4-IO27	63	64	JM4-IO58	A22	IO_L07N_0	I/O	0	VcccIO0
GND	GND	GND	-	-	GND	65	66	JM4-IO59	B23	IO_L07P_0	I/O	0	VcccIO0
VcccIO0	0	I/O	IO_L36N_0	B9	JM4-IO28	67	68	JM4-IO60	G17	IO_L08N_0	I/O	0	VcccIO0
VcccIO0	0	I/O	IO_L36P_0	A9	JM4-IO29	69	70	JM4-IO61	H17	IO_L08P_0	I/O	0	VcccIO0
VcccIO0	0	I/O	IO_L37N_0	D9	JM4-IO30	71	72	VccAux	-	-	out	VccAux	VccAux
VcccIO0	0	I/O	IO_L37P_0	E10	JM4-IO31	73	74	TDI	G7	TDI	JTAG	VccAux	VccAux
VcccIO0	0	I/O	IO_L38N_0	B8	JM4-IO32	75	76	TDO	E23	TDO	JTAG	VccAux	VccAux
VcccIO0	0	I/O	IO_L38P_0	A8	JM4-IO33	77	78	TCK	D4	TCK	JTAG	VccAux	VccAux
GND	GND	GND	-	-	GND	79	80	TMS	A25	TMS	JTAG	VccAux	VccAux

Pin-out of B2B connector JM4.

Connector JM5: Pin-Out Information

supply	bank	type	FPGA pin	FPGA ball	JM5 signal	JM5 pin	JM5 pin	JM5 singal	FPGA ball	FPGA pin	type	bank	supply
TE	-	in	-	-	Vb2b	1	2	Vb2b	-	-	in	-	TE
TE	-	in	-	-	Vb2b	3	4	Vb2b	-	-	in	-	TE
3.3V	1	I/O (I2C)	IO_L13P_1	Y22	SCL	5	6	/MR	-	-	in	-	3.3V
3.3V	1	I/O (I2C)	IO_L13N_1	Y23	SDA	7	8	/RESET	A2	PROG_B	in CONFIG	2	VccAux 3.3V
GND	GND	GND	-	-	GND	9	10	DONE	AB21	DONE	out CONFIG	VccAux	VccAux
3.3V	2	I/O DUAL	IO_L22N_2 DOUT	AE15	DOUT	11	12	SPI_D	AB15	IO_L30N_2 MOSI/CSI_B	SPI in DUAL	2	3.3V
3.3V	2	I/O DUAL	IO_L01N_2 M0	AD4	M0	13	14	INIT_B	AA15	IO_L34P_2 INIT_B	I/O DUAL	2	3.3V
3.3V	2	I/O DUAL	IO_L01P_2 M1	AC4	M1	15	16	Vsup	-	-	out	-	TE
3.3V	2	I/O DUAL	IO_L02P_2 M2	Y7	M2	17	18	SPI_Q	AF24	IO_L52P_2 D0/DIN/MISO	SPI out DUAL	2	3.3V
3.3V	2	I/O DUAL	IO_L07P_2 RDWR_B	Y12	RDWR _B	19	20	SPI_/S	AA7	IO_L02N_2 CSO_B	SPI out DUAL	2	3.3V
VccAux	VccAux	in CONFIG	PROG_B	A2	B2B _PROGB	21	22	SPI_/C	AE24	IO_L52N_2 CCLK	SPI out DUAL	2	3.3V
3.3 V	-	out	-	-	3.3V	23	24	D4	AE12	IO_L24N_2 D4	I/O DUAL	2	3.3V
3.3V	2	I/O PWRMGMT	IO_L22P_2 AWAKE	AD15	AWAKE	25	26	D5	AF12	IO_L24P_2 D5	I/O DUAL	2	3.3V
VccAux	VccAux	in PWRMGMT	SUSPEND	V20	SUSPEND	27	28	D6	AF10	IO_L22N_2 D6	I/O DUAL	2	3.3V
3.3V	2	I/O DUAL	IO_L36N_2 D1	AE18	D1	29	30	GND	-	-	GND	GND	GND
3.3V	2	I/O DUAL	IO_L36P_2 D2	AF18	D2	31	32	D7	AE10	IO_L22P_2 D7	I/O DUAL	2	3.3V
3.3V	2	I/O DUAL	IO_L34N_2 D3	Y15	D3	33	34	J5-IO20	AA18	IO_L47N_2	I/O	2	3.3V
3.3V	2	I/O GCLK	IO_L27P_2 GCLK0	Y14	J5-IO01	35	36	J5-IO21	AB18	IO_L47P_2	I/O	2	3.3V
GND	GND	GND	-	-	GND	37	38	J5-IO22	AE23	IO_L48N_2	I/O	2	3.3V
3.3V	2	I/O GCLK	IO_L28P_2 GCLK2	AF14	J5-IO02	39	40	J5-IO23	AF23	IO_L48P_2	I/O	2	3.3V
3.3V	2	I/O	IO_L29N_2	AC14	J5-IO03	41	42	J5-IO24	AE25	IO_L51P_2	I/O	2	3.3V
3.3V	2	I/O	IO_L39N_2	AE20	J5-IO04	43	44	1.2V	-	-	out	-	1.2 V
3.3V	2	I/O	IO_L39P_2	AF20	J5-IO05	45	46	J5-IO25	AF25	IO_L51P_2	I/O	2	3.3V
3.3V	2	I/O	IO_L40N_2	AC19	J5-IO06	47	48	J5-IO26	Y9	IO_L05N_2	I/O	2	3.3V
3.3V	2	I/O	IO_L40P_2	AD19	J5-IO07	49	50	J5-IO27	W9	IO_L05P_2	I/O	2	3.3V
GND	GND	GND	-	-	GND	51	52	J5-IO28	AF3	IO_L06N_2	I/O	2	3.3V
3.3V	2	I/O	IO_L41N_2	AC20	J5-IO08	53	54	J5-IO29	AE3	IO_L06P_2	I/O	2	3.3V
3.3V	2	I/O	IO_L41P_2	AD20	J5-IO09	55	56	J5-IO30	AF4	IO_L07N_2	I/O	2	3.3V
3.3V	2	I/O	IO_L42N_2	U16	J5-IO10	57	58	GND	-	-	GND	GND	GND
3.3V	2	I/O	IO_L42P_2	V16	J5-IO11	59	60	J5-IO31	AE4	IO_L07P_2	I/O	2	3.3V
3.3V	2	I/O	IO_L43N_2	Y17	J5-IO12	61	62	J5-IO32	AD6	IO_L08N_2	I/O	2	3.3V
3.3V	2	I/O	IO_L43P_2	AA17	J5-IO13	63	64	J5-IO33	AC6	IO_L08P_2	I/O	2	3.3V
2.5 V	-	out	-	-	2.5V	65	66	J5-IO34	W10	IO_L09N_2	I/O	2	3.3V
3.3V	2	I/O	IO_L44N_2	AD21	J5-IO14	67	68	J5-IO35	V10	IO_L09P_2	I/O	2	3.3V
3.3V	2	I/O	IO_L44P_2	AE21	J5-IO15	69	70	J5-IO36	Y13	IO_L25N_2 GCLK13	I/O GCLK	2	3.3V
3.3V	2	I/O	IO_L45N_2	AC21	J5-IO16	71	72	GND	-	-	GND	GND	GND
3.3V	2	I/O	IO_L45P_2	AD22	J5-IO17	73	74	J5-IO37	AA13	IO_L25P_2 GCLK12	I/O GCLK	2	3.3V
3.3V	2	I/O	IO_L46N_2	V17	J5-IO18	75	76	J5-IO38	AE13	IO_L26N_2 GCLK15	I/O GCLK	2	3.3V
3.3V	2	I/O	IO_L46P_2	W17	J5-IO19	77	78	J5-IO39	AF13	IO_L26P_2 GCLK14	I/O GCLK	2	3.3V
GND	GND	GND	-	-	GND	79	80	J5-IO40	W13	IO_L20N_2	I/O	2	3.3V

Pin-out of B2B connector JM5.

Signal Integrity Considerations

Traces of differential signals pairs are NOT routed symmetrically (as symmetric pairs).

Traces of differential signals pairs are NOT routed with equal length. For applications where traces length has to be matched or timing differences have to be compensated, The tables below list the trace length of I/O signal lines measured from FPGA balls to B2B connector pins.

Traces of differential signals pairs are routed with a differential impedance between the two traces of 60 ohm.

Pairs of pins that form a differential I/O pair appear colored together in the table. An electronic version of these pin-out tables are available for download from the Trenz Electronic support area of the web site.

Connector JM4: Signals Trace Lengths

len. mm	FPGA pin	FPGA ball	JM4 signal	JM 4 pin	JM 4 pin	JM4 signal	FPGA ball	FPGA pin	len. mm
				1	2				
26	IO_L20P_0	F15	JM4-IO01	3	4				
29	IO_L21N_0	C16	JM4-IO02	5	6				
				7	8	JM4-IO34	K12	IO_L39N_0	29
26	IO_L21P_0	D17	JM4-IO03	9	10	JM4-IO35	J12	IO_L39P_0	26
24	IO_L22N_0	C15	JM4-IO04	11	12	JM4-IO36	D8	IO_L40N_0	26
26	IO_L22P_0	D16	JM4-IO05	13	14	JM4-IO37	C8	IO_L40P_0	24
21	IO_L23N_0	A15	JM4-IO06	15	16				
20	IO_L23P_0	B15	JM4-IO07	17	18	JM4-IO38	C6	IO_L41N_0	24
22	IO_L24N_0	F14	JM4-IO08	19	20	JM4-IO39	B6	IO_L41P_0	24
18	IO_L24P_0	E14	JM4-IO09	21	22	JM4-IO40	C7	IO_L42N_0	23
				23	24	JM4-IO41	B7	IO_L42P_0	19
20	IO_L25N_0 GCLK5	J14	JM4-IO10	25	26	JM4-IO42	K11	IO_L43N_0	24
21	IO_L25P_0 GCLK4	K14	JM4-IO11	27	28	JM4-IO43	J11	IO_L43P_0	23
11	IO_L26N_0 GCLK7	A14	JM4-IO12	29	30				
11	IO_L26P_0 GCLK6	B14	JM4-IO13	31	32	JM4-IO44	D6	IO_L44N_0	15
17	IO_L27N_0 GCLK9	G13	JM4-IO14	33	34	JM4-IO45	C5	IO_L44P_0	14
16	IO_L27P_0 GCLK8	F13	JM4-IO15	35	36	JM4-IO46	B4	IO_L45N_0	15
				37	38	JM4-IO47	A4	IO_L45P_0	14
13	IO_L28N_0 GCLK11	C13	JM4-IO16	39	40	JM4-IO48	H10	IO_L46N_0	14
12	IO_L28P_0 GCLK10	B13	JM4-IO17	41	42	JM4-IO49	G10	IO_L46P_0	14
14	IO_L29N_0	B12	JM4-IO18	43	44				
14	IO_L29P_0	A12	JM4-IO19	45	46	JM4-IO50	H9	IO_L47N_0	15
27	IO_L30N_0	C12	JM4-IO20	47	48	JM4-IO51	G9	IO_L47P_0	14
30	IO_L30P_0	D13	JM4-IO21	49	50	JM4-IO52	E7	IO_L48N_0	13
				51	52	JM4-IO53	F7	IO_L48P_0	15
20	IO_L33N_0	B10	JM4-IO22	53	54	JM4-IO54	B3	IO_L51N_0	9
17	IO_L33P_0	A10	JM4-IO23	55	56	JM4-IO55	A3	IO_L51P_0	9
20	IO_L34N_0	D10	JM4-IO24	57	58				
21	IO_L34P_0	C10	JM4-IO25	59	60	JM4-IO56	C23	IO_L06N_0	36

29	IO_L35N_0	H12	JM4-IO26	61	62	JM4-IO57	D23	IO_L06P_0	42
30	IO_L35P_0	G12	JM4-IO27	63	64	JM4-IO58	A22	IO_L07N_0	36
				65	66	JM4-IO59	B23	IO_L07P_0	41
27	IO_L36N_0	B9	JM4-IO28	67	68	JM4-IO60	G17	IO_L08N_0	36
27	IO_L36P_0	A9	JM4-IO29	69	70	JM4-IO61	H17	IO_L08P_0	39
28	IO_L37N_0	D9	JM4-IO30	71	72				
34	IO_L37P_0	E10	JM4-IO31	73	74				
29	IO_L38N_0	B8	JM4-IO32	75	76				
28	IO_L38P_0	A8	JM4-IO33	77	78				
				79	80				

Trace length of signal pins of B2B connector JM4

Connector JM5: Signals Trace Lengths

len. mm	FPGA pin	FPGA ball	JM5 singal	JM5 pin	JM5 pin	JM5 singal	FPGA ball	FPGA pin	len. mm
				1	2				
				3	4				
				5	6				
				7	8				
				9	10				
21	IO_L22N_2 DOUT	AE15	DOUT	11	12	SPI_D	AB15	IO_L30N_2 MOSI/CSI_B	51
35	IO_L01N_2 M0	AD4	M0	13	14	INIT_B	AA15	IO_L34P_2 INIT_B	51
49	IO_L01P_2 M1	AC4	M1	15	16				
49	IO_L02P_2 M2	Y7	M2	17	18	SPI_Q	AF24	IO_L52P_2 D0/DIN/MISO	52
23	IO_L17P_2 RDWR_B	Y12	RDWR _B	19	20	SPI_/S	AA7	IO_L02N_2 CSO_B	95
				21	22	SPI_/C	AE24	IO_L52N_2 CCLK	75
				23	24	D4	AE12	IO_L24N_2 D4	14
10	IO_L22P_2 AWAKE	AD15	AWAKE	25	26	D5	AF12	IO_L24P_2 D5	13
				27	28	D6	AF10	IO_L22N_2 D6	15
7	IO_L36N_2 D1	AE18	D1	29	30				
7	IO_L36P_2 D2	AF18	D2	31	32	D7	AE10	IO_L22P_2 D7	16
13	IO_L34N_2 D3	Y15	D3	33	34	J5-IO20	AA18	IO_L47N_2	22
13	IO_L27P_2 GCLK0	Y14	J5-IO01	35	36	J5-IO21	AB18	IO_L47P_2	16
				37	38	J5-IO22	AE23	IO_L48N_2	20
9	IO_L28P_2 GCLK2	AF14	J5-IO02	39	40	J5-IO23	AF23	IO_L48P_2	23
12	IO_L29N_2	AC14	J5-IO03	41	42	J5-IO24	AE25	IO_L51P_2	26
17	IO_L39N_2	AE20	J5-IO04	43	44				
19	IO_L39P_2	AF20	J5-IO05	45	46	J5-IO25	AF25	IO_L51P_2	34
21	IO_L40N_2	AC19	J5-IO06	47	48	J5-IO26	Y9	IO_L05N_2	20

22	IO_L40P_2	AD19	J5-IO07	49	50	J5-IO27	W9	IO_L05P_2	20
				51	52	J5-IO28	AF3	IO_L06N_2	10
27	IO_L41N_2	AC20	J5-IO08	53	54	J5-IO29	AE3	IO_L06P_2	11
26	IO_L41P_2	AD20	J5-IO09	55	56	J5-IO30	AF4	IO_L07N_2	11
27	IO_L42N_2	U16	J5-IO10	57	58				
30	IO_L42P_2	V16	J5-IO11	59	60	J5-IO31	AE4	IO_L07P_2	17
36	IO_L43N_2	Y17	J5-IO12	61	62	J5-IO32	AD6	IO_L08N_2	21
36	IO_L43P_2	AA17	J5-IO13	63	64	J5-IO33	AC6	IO_L08P_2	26
				65	66	J5-IO34	W10	IO_L09N_2	31
44	IO_L44N_2	AD21	J5-IO14	67	68	J5-IO35	V10	IO_L09P_2	38
39	IO_L44P_2	AE21	J5-IO15	69	70	J5-IO36	Y13	IO_L25N_2 GCLK13	43
43	IO_L45N_2	AC21	J5-IO16	71	72				
47	IO_L45P_2	AD22	J5-IO17	73	74	J5-IO37	AA13	IO_L25P_2 GCLK12	40
44	IO_L46N_2	V17	J5-IO18	75	76	J5-IO38	AE13	IO_L26N_2 GCLK15	32
45	IO_L46P_2	W17	J5-IO19	77	78	J5-IO39	AF13	IO_L26P_2 GCLK14	35
				79	80	J5-IO40	W13	IO_L20N_2	44

Trace length of signal pins of B2B connector JM5