TE0300 FPGA User I/Os

A total of 110 FPGA user I/Os are available on corresponding contacts of B2B connectors J4 and J5 (see here).

- 37 differential digital I/O pairs:each pair is configurable as 2 single-ended digital I/Os, corresponding to a maximum of 74 single-ended digital I/Os;
- 4 differential clock input pairs:each pair is configurable as differential digital I/O pair or 2 single-ended clock inputs or 2 single-ended digital I/Os (or combination thereof), corresponding to from a maximum of 8 independent clock inputs to a maximum of 8 independent digital I/Os;
- 1 differential clock input pair:the pair is configurable as differential digital input pair or as 2 single-ended clock inputs or 2 single-ended digital inputs (or combination thereof), corresponding to from a maximum of 2 independent clock inputs to a maximum of 2 independent digital inputs;
- 21 single-ended digital I/Os;
- 5 single-ended inputs.

The table below summarizes the maximum available FPGA user I/Os divided by supply voltage.

type	VccIO	3.3 V
diff. I/O pairs	18	23
diff inputs	1	none
diff. clocks	4	1
s. e. I/Os	46	58
s. e. inputs	2	4
s. e. clocks	8	3

Maximum FPGA user I/Os by supply voltage.

Differential signal pairs

The micromodule has a total of 42 differential signal pairs routed pairwise with a differential impedance of 100 ohm to adjacent connector pins. These lines can be used for high speed signaling up to 666 Mbit/s per differential pair (see Xilinx Application Note XAPP485).