TE0300 DIP Slide Switch S4 (Configuration)

S4 enables / disables the FPGA configuration through the SPI interface. The FPGA configuration through the JTAG interface cannot be disabled.
When S4 is turned on, the FPGA tries to configure from the SPI Flash memory. The FPGA can be configured by the JTAG interface at any time.
When S4 is turned off, the FPGA waits to be configured by the JTAG interface.
For further information about direct (pure SPI) / indirect (SPI over JTAG) in-system programming of SPI flash memories, please see Xilinx Application Notes XAPP951 "Configuring Xilinx FPGAs with SPI Serial Flash" and XAPP974 "Indirect Programming of SPI Serial Flash PROMs with Spartan-3A FPGAs".

S4	label	position
ON*	SPI	FPGA configuration: JTAG + SPI
OFF	JTAG	FPGA configuration: JTAG

S4 (*default: ON).

When downloading via parallel JTAG programmer to FPGA, it can happen that programming fails with Error: "*'1' : Programming terminated. DONE did not go high.*" Try setting DIP switch S4 to JTAG-only. A bug in certain Xilinx iMPACT versions can cause this.