TE0630 FPGA Configuration Using SPI Indirect In-System Programming (ISP)

DIP Switches Configuration is not required

Similar to the traditional configuration memories, SPI serial Flash memories must be loaded with the configuration data. SPI serial Flash memories have a single interface for programming, but there are multiple methods to deliver the data to this interface. These sections describe the hardware setup, the PROM file generation flow and the software flow for ISP (indirect in-system programming) of a Trenz Electronic TE0630 SPI serial Flash configuration PROM through the JTAG interface of a Xilinx Spartan-6 FPGA using Xilinx iMPACT 11.5 (with other version the procedure should be almost the same).

To write the SPI Flash memory, perform the steps of this page.