TE0630 Board revisions and assembly variants

To determine PCB revision and assembly variant from FPGA, TE0630 have dedicated user signals, which can be read by user core.
Board revision coded in 4 bits BR[3:0]

Signal name	FPGA pin
BR0	R19
BR1	V19
BR2	V20
BR3	T17

Board revision pins

To define low (zero) level BR pin connected to ground rail, to define high (one) level BR pin left float (open). These pins should be configured with "pullup" option in user design.
See the table above for current list of board revisions.

BR3	BR2	BR1	BR0	
0	0	0	0	00 Initial revision

Board revisions

Module assembly variant encoded using AV[3:0] pins.

Signal name	FPGA pin
AV0	Y20
AV1	R15
AV2	R16
AV3	R17

Assembly variants pins

To define low (zero) level AV pin connected to ground rail through zero resistor, to define high (one) level AV pin left float (open). These pins should be configured with "pullup" option in user design.
Available module assembly variants listed in the table below.

AV3	AV2	AV1	AV0	
0	0	0	0	Base assembly variant

Module assembly variants