TE0300 Power Supply

The module can be powered by the B2B connector or the USB connector. If both power supplies are available, the **B2B connector power supply takes precedence**, disabling the USB power supply automatically.

Power Supply Range

TE0300 requires only one power supply with a supply voltage between 4.0 V and 5.5 V. Power consumption depends on the active design.

On-board Power Rails

Three on-board voltage regulators provide the following power supply rails needed by the components on the micromodule:

- 1.2 V, 1 A max
- 2.5 V, 1 A max
- 3.3 V, 1 A max

The power rails are available for the FPGA and can be shared with a baseboard by the **corresponding** lines of the B2B connectors J4 and J5.

> ⚠ Please note that the **power consumption of the FPGA is highly dependent on the design** actually loaded. So please use a tool like Xilinx Xpower to determine the expected power consumption.

> ⚠ Even if the provided voltages of the module are not used on the baseboard, it is recommended to bypass them to ground with 10 nF - 100 nF capacitors

USB Power Supply

The module is powered by the USB connector if the following conditions are met:

- the module is equipped with an USB connector,
- the module is connected to a USB bus,
- no power supply is provided by the B2B connectors.

In this case, other components (e.g. extension or carrier boards) may also be powered by the corresponding 5 Volt line (5V) of the B2B connector J5.

B2B Connector Power Suplly

The B2B connector power supply requires a single nominal 5 V DC power supply. The power is usually supplied to the module through the 5 V contacts (5Vb2b) of the B2B connectors J5 (see here). The recommended minimum supply voltage is 4 V. The maximum supply voltage is 5.5 V. The recommended maximum continuous supply current is 1.5 A.

I/O Bank Power Supply

The Spartan-3E architecture organizes I/Os into four I/O banks (see the table below).

Bank	SupplyVoltage (V)	Min(V)	Max(V)
B0	VccIO	1.2	3.3
B1	2,5	-	-
B2	3,3	-	-
B3	3,3	-	-

I/O banks power supply

Voltage for banks B1, B2 and B3 is fixed respectively to 2,5 V, 3,3 V and 3,3 V.
Voltage VccIO for bank B0 shall span from 1.2 V to 3.3 V. VccIO can be supplied either externally or internally to the micromodule.

> ⊙ Spartan-3 I/Os are not 5 V tolerant. Applying more than the recommended operating voltages at any pin, results in a damaged FPGA (see Xilinx Answer AR#19146).

🛑

Externally Supplied VccIO

VccIO can be externally supplied over the B2B connector J4. If bank B0 is not used, then VccIO can be left open.

Internally Supplied VccIO

If VccIO is **not** externally supplied, it can be internally supplied by **one** of the internal power rails of 2.5 V and 3.3 V. This is possible by short-circuiting **one** of the two pad pairs placed on the right of connector J4 at the top right corner of the bottom side of the micromodule.

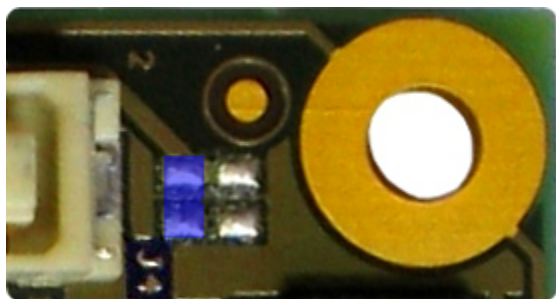Two suitable ways of shirt-circuiting the paid pair are by means of

- a zero-ohm 0603 (1608 metric) chip resistor or
- a solder blob.

This figure shows how to short-circuit VccIO to internal 3.3 V power rail.
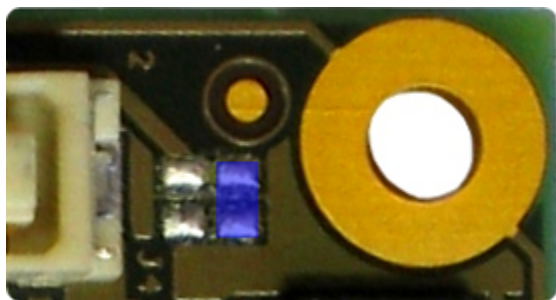
R102 pad pair (blue highlight) for 3.3 V internal supply.

This figure shows how to short-circuit VccIO to internal 2.5 V power rail.

R103 pad pair (blue highlight) for 2.5 V internal supply.