


TE0320 USB Interface

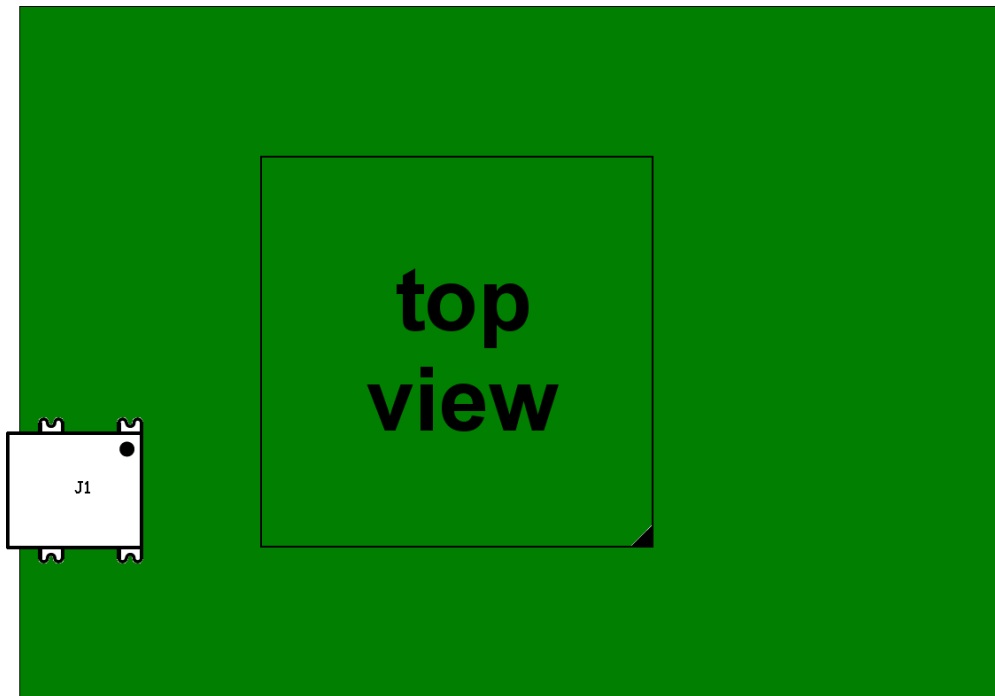
USB communication can be performed in one of the following two ways:

- through a USB connector
- through USB lines at one B2B connector.

 Only one connection type at one time is allowed.

USB Connector

TE0320 is provided with a USB mini-B receptacle (device) connector J1 on the top side.



USB connector (top view).

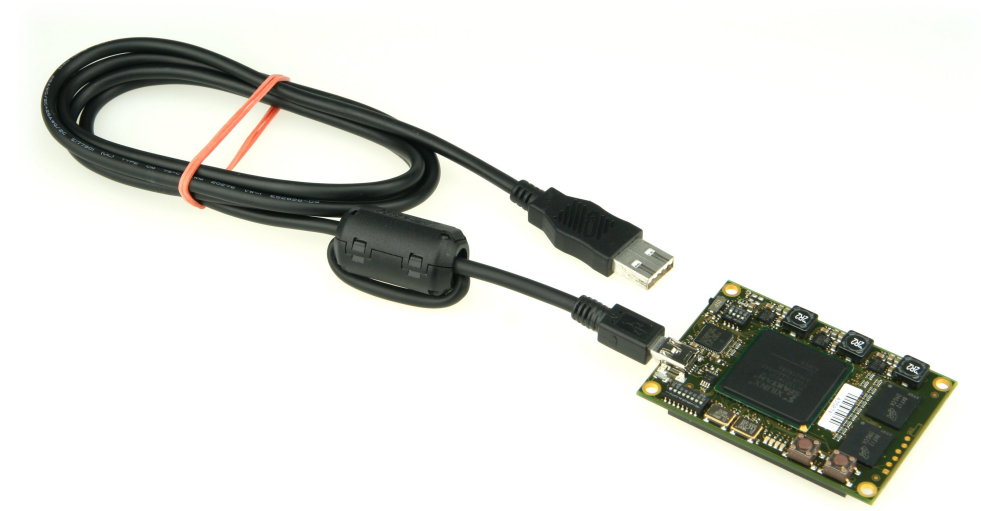


USB mini-B receptacle (device) connector.


The figure below shows a sample USB connection between computer and TE0320 for both configuration and operation. The USB cable provides for

- Power supply.
- Configuration by means of the Firmware Upgrade Tool (FUT), recommended for field upgrades. Please use a dedicated JTAG Adapter during development.

- Data communication channel during operation.



Sample USB connection (TE0320 side).

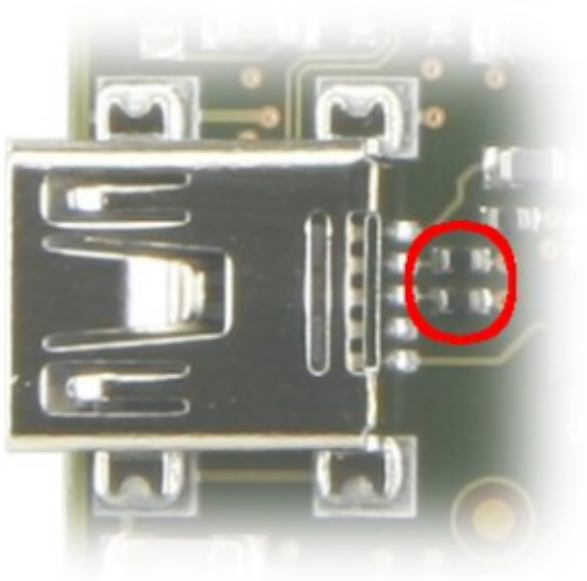
 Should you require a module version without connector J1, please contact Trenz Electronic.

USB Pins

USB communication can be performed over 2 pins of B2B connector JM4 as detailed in Table 3. Ensure resistors R3 and R4 are populated to connect USB B2B pins B2B_D_P and B2B_D_P to USB lines D_P and D_P respectively.

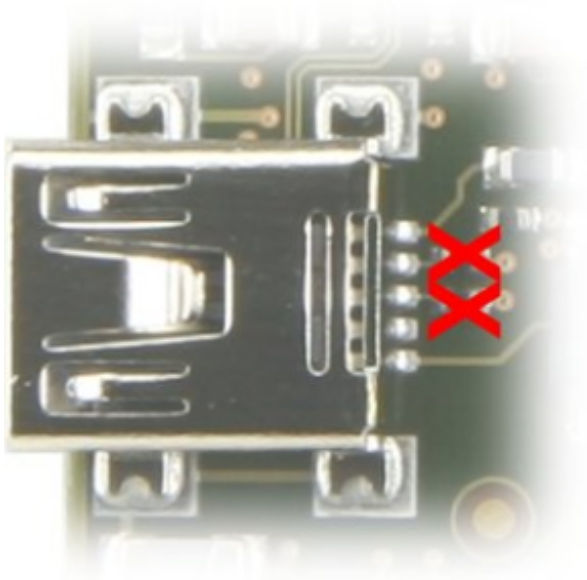
pin number	pin name	signal name	description
4	B2B_D_P	D_P	USB data + (D+)
6	B2B_D_N	D_N	USB data - (D-)

USB pins at B2B connector JM4.



Resistors R3 and R4 required for USB communication over B2B connector JM4.

In order to minimize the stub on USB lines and improve communication quality, the connection to both USB pins of B2B connector JM4 can be interrupted by removing resistors R3 and R4.



Resistors R3 and R4 removed for lower stub on USB lines.

TE0320 USB Controller

TE0320 is equipped with a Cypress EZ-USB FX2 controller to provide a high-speed USB 2.0 interface. The controller uses 4 interfaces (see [here](#)):

- USB interface (to USB connector);
- I²C interface (to EEPROM);

- SPI interface (to FPGA and Flash);
- FIFO interface (to FPGA).

The I²C interface connects the USB controller to the EEPROM chip, which stores vendor ID and device ID. See [chapter DIP Switch](#) for available options.
The SPI interface is used to communicate with the FPGA and to access the SPI serial Flash chip.
The FIFO interface provides a high-speed communication channel with the FPGA. The interface can transfer up to 48 MB/s burst rate.