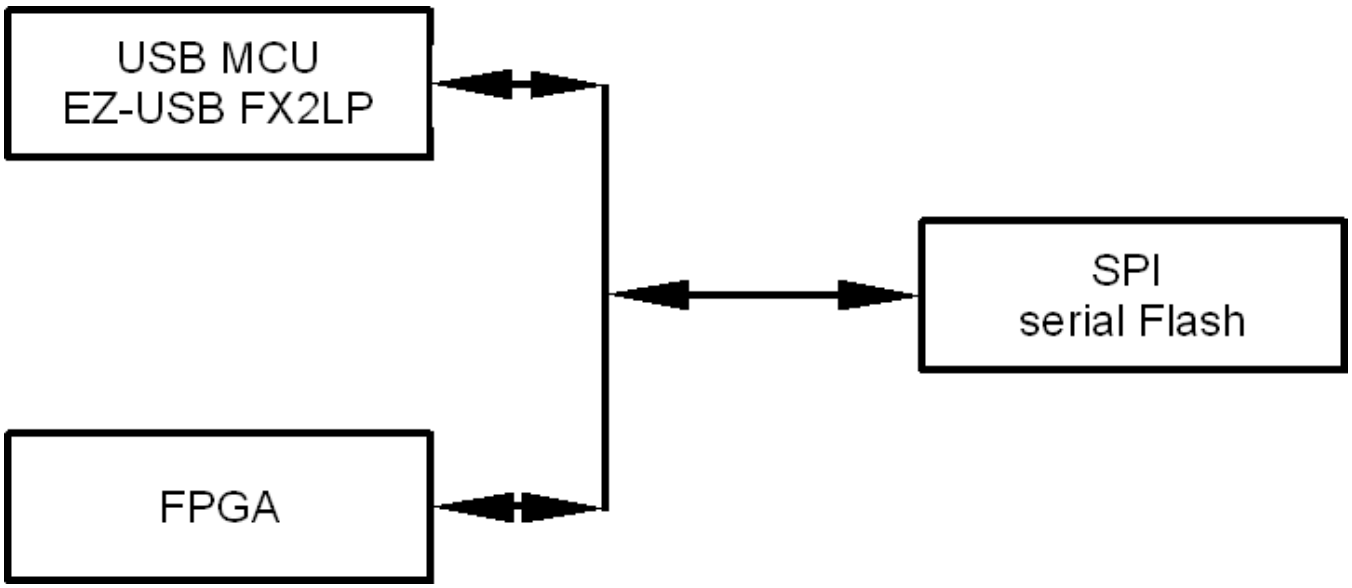
TE0630 SPI bus

TE0630 has a flexible SPI bus on-board as outlined in the figure below.



SPI bus topology.

SPI signals on the TE0630 are listed and described in the table below.

name	definition	description
SPI_Q	serial data output	This output signal is used to transfer data serially out of the device. Data is shifted out on the falling edge of SPI_/C.
SPI_D	serial data input	This input signal is used to transfer data serially into the device. It receives instructions, addresses, and the data to be programmed. Values are latched on the rising edge of SPI_/C
SPI_/C	serial clock	This input signal provides the timing of the serial interface. Instructions, addresses, or data present at SPI_D are latched on the rising edge of SPI_/C. Data on SPI_Q changes after the falling edge of SPI_/C.
SPI_/S	chip select	When this input signal is **high,** the device is **disabled** and SPI_Q is at high impedance (Z).
		When this input signal is **low**, the device is **enabled.**
		After power-up, a falling edge on SPI_/S is required prior to the start of any instruction to the Flash memory.

SPI signals summary.

SPI signals are routed to / from bank 2 of the FPGA of the TE0630 is as detailed in the table below.

name	FPGA pin	J5 pin
SPI_Q	IO_L03N_2	no
SPI_D	IO_L16N_2	no

SPI_/C	IO_L26N_2	no
SPI_/S	IO_L01P_2	no

SPI pin-out summary; SPI signal details (bank 2).

The SPI bus can be used during configuration and operation in a plurality of ways as summarized respectively in Table A (SPI bus for configuration) and Table B (SPI bus for operation).

> Any other usage of the SPI bus is neither supported nor recommended.

SPI bus for configuration

The SPI bus is used for configuration in two ways by default:

1. EZ-USB â-º Flashthe USB FX2 microcontroller (master) writes the PROM file (containing the FPGA configuration bitstream) to the SPI serial Flash memory (slave)
2. FPGA â—„ Flashthe FPGA (master) configures itself in Master SPI mode from the SPI serial Flash memory (slave).

In case (a), the FPGA shall be turned off to release its shared SPI pins.
In case (b), the USB FX2 microcontroller shall three-state (Z = high impedance) its shared SPI pins.

description	usage	EZ-USB FX2LP	FPGA	B2B J5	serial Flash
EZ-USB â-º Flash	OpenFUT API	**master**	off (S3 = FX2PON, FX2_PS_EN = 0)	deselected	slave
FPGA â—„ Flash	OpenFUT API	inactive SPI_* = Z	**master** (SPI_/S = 1)	deselected	slave

Table A: SPI bus modes for configuration.

SPI bus for operation

A plurality of usage combinations of the SPI bus during operation is made available to the user as suggested in Table B below.

description	usage	EZ-USB FX2LP	FPGA	B2B J5	serial Flash
EZ-USB â—„â-º Flash	custom	**master**	off (S3 = FX2PON, FX2_PS_EN = 0)	deselected	slave
FPGA â—„â-º Flash	custom	inactive SPI_* = Z	**master** (SPI_/S = 1)	deselected	slave

Table B: SPI bus modes for operation.

> Other combinations of master and slave units are neither supported nor recommended.