Changes from TE0300-00 to TE0300-01

Clocks

TE0300-00 has a 50MHz secondary clock, whereas TE0300-01 has a 125MHz secondary clock.

B2B Connectors

Contact 14 of connector J5 has been extended from an input in TE0300-00 to an I/O in TE0300-01. Therefore hardware designs developed for the TE0300-00 are compatible with the TE0300-01 whereas those developed for the TE0300-01 are compatible with the TE0300-00 if that contact is configured as input.

Contact 76 of connector J5 has mistakenly been described as I/O in TE0300-00, but it has always been an input-only contact as documented for TE0300-01.

Connector J4 has not been changed.

LED0

With TE0300-00, the LED is lit when the U_LED line on pin T15 is set high whereas with TE0300-01 the LED is lit when the U_LED line on pin R10 is set high.

Volatile Memory Interface

TE0300-00 could access the DDR SDRAM *only* with Xilinx OPB (on-chip peripheral bus) cores.
TE0300-01 can *also* access the DDR SDRAM through the dedicated Xilinx MIG (memory interface generator) memory interface.