Update the XPS project

Double click "set_0xxx_project.bat" to select the corresponding FPGA mounted on TE USB FX2 module.

Double click the "system.xmp" in "C:\XilinxProject\reference-TE0xxx".

The Xilinx Platform Studio should open.

You should click "Project" and then click "Project Options".

8 File Edit View					
-	Project Hardware Device Configuration Debug Sin	ulation Window Help	p		- 4
	Project Options				
	Design Rule Check Ctrl+Shift+D	Ports Addresses			(9)
Navigator 🎽		Ports Houreases	10.7	TO 14	<u></u>
Design Flow	Select Elf File	BusiName	и туре	IP version	
beaginion	Export Hardware Design to SDK		Imb_v10	1.00.a	
	~	-	a nho_vio	105.8	
×	Archive Project		t microblaze	7.30.b	
Run DRCs	DQ Generate Block Diagram Image (Obsolete)		fram_block	1.00.a	
			Imb_bram_if_cntlr	2.10.b	
Implement Flow	Copen Graphical Design View		Imb_bram_if_cntlr	2.10.b	
Implement how	Generate and View Design Report		mpmc	6.06.a	
€ 1	😰 View Design Summary		4 mdm	1.00.g	
		-	Tr xps_intc	2.01.a	
Generate Netlist	Run Version Migration		trans anio	2.00.a	
	🚱 Rescan User Repositories		mark xps i2c slave	1.20.a	
*	🗸 Launch Xilinx Shell		🙀 xps_npi_dma	3.00.a	
1010	Customize Buttons		🚖 xps_spi	2.02.b	
Generate BitStream			🙀 xps_timer	1.02.a	
	Clean All Generated Files		🙀 xps_uartlite	1.02.a	
	Terminate Running Process	F	Tr clock_generator	4.03.a	
- COURS	in the second se	at 0	W util_reduced_logic	200.5	
Export Design					
Launch Simulator					
	Legend Master Slave Master/Slave Target (Initiator) Moroduction Cucense (paid) Cucense (eval)	Connected OUnconnecte	d M Monitor RBeta ZDevelopment		

XPS: Project>Project Options

Under "Advanced Options (Optional) > Project Peripheral Repository Search Path" you must write (if it is not already written) "..TE-EDK-IP\".

eneral	Design Flor	W					
Target D	evice						
Archited	ture	Device Size		Package		Speed Gra	ade
spartar	n3e 💌	xc3s1600e		fg320	•	-4	
Advance Project	d Options (Options (Options Re Peripheral Re DK-IP\	otional) pository Search	Path			B	rowse
Advance Project \TE-E Custom	ed Options (Op Peripheral Re DK-IP\ Makef <mark>Enter</mark>	otional) pository Search a semicolon se	Path parated	d list of direct	ories.	B	rowse

You should not alter folder nesting or select MyProcessorIPLib because double nesting of folders is a Xilinx Platform Studio requirements.



After this selection the XPS should appear like in this image.



XPS project to start

Now, you can cancel (or move in another folder) the content of "TE0xxx-Reference-Designs\reference-TE0xxx\SDK\SDK_Export".

You can copy all .c and .h files from "TE0xxx-Reference-Designs\reference-TE0xxx\SDK\SDK_Workspace\demo\src" in a temporary folder ("C: \demo_src_TE" for example).

You can cancel all files and folders from "TE0xxx-Reference-Designs\reference-TE0xxx\SDK\SDK_Workspace".

⁽¹⁾xxx is

- 300 for TE0300 project: TE0300 project and TE0320 project are contained in the same folder TE03xx
 320 for TE0320 project. TE0300 project and TE0320 project are contained in the same folder TE03xx
- 630 for TE0630 project