

System Components

Host PC

Cypress FX2 microcontroller firmware implement standard USB CDC interface which can be easily managed by most modern OS. OS define this interface as serial (COM) port. Microsoft Windows OS require Cypress COM port driver, which can be easily archived and installed. For example [Cypress AN58764](#) contain Virtual COM port driver "inf" file. Usual COM port have several options (baudrate, parity, stop bits, and others) related to RS protocol and generic serial port controllers management. Virtual COM port don't need this options for work, so it can be used for other purposes.

Cypress FX2 microcontroller

FX2 microcontroller implement USB CDC class interface, which include 3 endpoints (control endpoint and 2 data endpoints). By default data endpoints configured in "AutoIn" and "AutoOut" modes to transfer data to and from FPGA interface. User can switch microcontroller firmware to CLI, EEPROM or Flash management mode, in this case out endpoints will be reconfigured to manual mode and data from host processed by microcontroller firmware.

FPGA project

FPGA project communicate with FX2 microcontroller using 8-bit synchronous Slave FIFO interface. All signals configured to active high level. When Host PC send data to COM port it comes to FX2 EP2 FIFO. FPGA project can read data from EP2, process it and write to EP6 FIFO. EP2 and EP6 FIFOs size is 512 bytes, quad buffered. FPGA project should check FIFOs flags.

Signal	FX2 Flag	Description
FlagA	EP2EF	Receive FIFO empty flag. '1' When EP2 FIFO empty.
FlagB	EP6FF	Transmit FIFO full. '1' When EP6 FIFO full.
FlagC	EP6PF	Transmit FIFO almost full. '1' when less than 128 bytes free in EP6 FIFO.
FlagD	EP2PF	Receive FIFO almost full. '1' when more than 128 bytes in EP2 FIFO.

Flags description