PROM file from the bitstream file (XILINX Flash .mcs example)

In order to generate a .mcs PROM file from the bitstream file download.bit, start Xilinx iMPACT. The following example shows the case of Xilinx iMPACT 11.3 (for other version the procedure doesn't change):

🐉 New iMPACT Project	Select "file / new project".
I want to	Choose "create a new project".
O load most recent project	Press " OK" .
Load most recent project file when iMPACT starts	
create a new project (.ipf) default.ipf Browse	
<u>O</u> K <u>C</u> ancel	

Section 2017	Select "prepare a PROM file".
Please select an action from the list below	Press " OK ".
Configure devices using Boundary-Scan (JTAG)	
Automatically connect to a cable and identify Boundary-Scan chain	
Prepare a PROM File	
O Prepare a System ACE File	
O Prepare a Boundary-Scan File	
SVF 🗸	
Configure devices using Slave Serial mode	
OK Cancel	

New iMPACT Project

Select step 1. "storage target / Xilinx Flash/PROM" of the left panel and press the left green arrow.

PROM File Formatter								×
Step 1. Select Storage Target		Step 2. Add	Storage Device(s)		Step 3,		Enter Da	ata
Storage Device Type :					General File Detail		Value	
Xilinx Flash/PROM		Storage Device (bits):	512K		Checksum Fill Value	FF		
General Spartan SAN		Add Storage Device	Remove Storage Device		Output File Name	Untitled		
Configure Single FPGA					Output File Location	C:\Xilinx\		B
- Configure Single FPGA					Flash/PROM File	e Property	Value	
Configure from Paralleled PROMs					File Format		HEX	
					Use Power-of-2 for	Start Addr	No	
					Number of Bitstrear	m	2	
					Bitstream 0 Start A	ddress	0	
					Bitstream 1 Start A	ddress	675840	
					Add Non-Configura	tion Data Files	Yes	
					Number of Data File	e		
		Auto Select PROM			<			Σ
Description:								
The PROM File Formatter will guide you through the steps to format bitstream BIT files into a PROM file that is compatible with Xilinx® and third-party PROM programmers. The programmed PROM device can then be used to configure the target FPGA.								
Additional capabilities of the PROM File Formatter include	:							
Generation PROM files containing specific EPGA	oofigura	tion instructions required to	sunnort daisv-chained EPGA hi	itstream	BIT files.			~
					ОК	Can	cel Help	

PROM File Formatter Step1

Select step 2. "add storage device(s) / auto select PROM" of the middle panel and press the right green arrow.

In step 3. "enter data" of the right panel

PROM File Form	natter										
Step 1.	Select Storage Target		Step 2,	Add	Storage	e Device(s)		Step 3.		Enter D)ata
Storage Device Type	:		BD OM Esculu		Distform E	ach M		General File Detail		Value	
Xilinx Flash/PROM	4 A		Device (bits)		xcf01s	[1 M]		Checksum Fill Value	FF		
Spartan3AN			Add Storage De	evice	Remove S	torage Device		Output File Name	Untitled		
Configure Si	ngle FPGA ultiBoot FPGA			01100				Output File Location	C:\Xilinx\		Þ
Configure Si	ngle FPGA ultiBoot FPGA							Flash/PROM Fi	le Property	Value	
Generic Parallel F	om Paralleled PROMs PROM							File Format		MCS	~
								Enable Revisioning		Yes	\sim
								Number Of Revisio	ns		\sim
								Enable Compressio	n	No	~
			Auto Select PF	ROM							
Description:											
In this step, you will • Checksum • Output File • Output File • File Formal	enter information to assist in setting Fill Value: When data is insufficient Name: This allows you to specify th Location: This allows you to specif : PROM files can be generated in an	up and g to fill the e base r / the dire / numbe	enerating a PROM fi ane of the file to wl actory in which the fi r of industry standar	ile for the PROM, I hich your ile named rd formal	e targeted s the value sp PROM data d above will s. Denendir	torage device an ecified here is us a will be written be created na on the PROM f	d mode. ed to ca ile forma	culate the checksur t your PROM progra	n of the unuse	d portions. ou outout a TEK. ncel Hi	

PROM File Formatter Step 3

 ${}_{\oslash}$

Type *fpga* (or another name) in the "Output File Name" input field

Using OpenFut or OpenFutNet, there is no longer any restriction in the name of output file: any name for the output file name input field is allowed.

With the old 2nd generation program FWU any other name than *fpga* for the output file name input field is <u>not</u> allowed.

Choose a suitable path for the "Output File Location" input field;

Select mcs from the drop-down menu file format in the flash/PROM file property sub-panel;

PROM File Formatter							
Step 1. Select Storage Targe	t	<i>Step 2.</i> A	dd Storage Device(s)		Step 3,		Enter Data
Storage Device Type :		DROM Family	Dia Manager Claude		General File Detail		Value
Xilinx Flash/PROM		Device (bits)	xcf01s [1 M]		Checksum Fill Value	FF	
Spartan3AN ⊡ SPI Flash		Add Storage Device	Remove Storage Device		Output File Name	fpga	
Configure Single FPGA					Output File Location	C:/Daten	>
Configure Single FPGA					Flash/PROM Fil	e Property	Value
Configure from Paralleled PROMs					File Format		BIN (Swap Bits ON) 🔽
					Enable Revisioning		MCS
					Number Of Revision	าร	TEK
					Enable Compressio	n	HEX (Swap Bits ON) HEX (Swap Bits OEE)
							BIN (Swap Bits ON)
							BIN (Swap Bits OFF) UFP ('C' format)
							ISC
		🗹 Auto Select PROM					
Description:	-						
In this step, you will enter information to assist in setting	up and o	enerating a PROM file fo	r the targeted storage device and	i mode.			~
• Charlieum Fill Yaluar When data is insufficier	r ta fill th	o optivo momoru of o DDC	M the value specified here is use	d to co	kulato the checkeum	of the upuse	d portions
• Output File Name: This allows you to specify	he base i	name of the file to which	your PROM data will be written	utota	culate the checksun	i or the anase	a portions. —
Output File Location: This allows you to spece File Format: PROM files can be generated in a	fy the dir	ectory in which the file na r of industry standard fo	amed above will be created rmats. Depending on the PROM fil	e forma	t your PROM progra	mmer lises i vi	ou outout a TEK 🛛 💌
	1. 1. 1. 1. 1. 1.						

Prom File Formatter Step 3, MCS selection

Press the "OK" button in the bottom left corner of the current window.

😺 Add I	Device 🛛 🔀	Just acknowledge the pup-up message.
٩	Start adding device file to Revision: 0	
	ОК	

Add Device Suchen in: implementation Implementatio	Browse to the "./implementation/" folder of your "." project folder and select the bitstream file download. bit. Press the "open" button in the bottom left corner of the current window.
Add Device Image: Comparison of the tote of tote	Your design likely consist of just one device file. So deny the request by pressing the " NO " button.
Add Device Image: Complete the device file entry. Vou have completed the device file entry. Click 'Ok' to continue OK OK	Just acknowledge the pup-up message.

PROM File Formatter after Step 3

Select "operations / generate file..." or double click "generate file..." from the iMPACT processes panel.

🐉 ISE iMPACT - [PROM File Formatter: Xi	(ilinx Flash/PROM]	
🛞 File Edit View Operations Output De	Debug Window Help	_ 8 ×
🗄 🗋 🎓 📑 🕴 🔏 🛛 Access eFUSE Register	ers 🕨 🔟 📝 🍂 🎼	
iMPACT Flows Generate File		^
Boundary Scan SlaveSerial Direct SPI SystemACE Create PROM File (PROM File Formatter) IMPACT Processes ↔ □ ♬ × Available Operations are: → Generate File		•
	PROM File Formatter: Xilinx Flash/PROM	
Console		⇔⊡₽×
<pre>INFO::MPACT:501 - '1': Added Add one device.fa361</pre>	Device xc3sd1800a successfully.	× .
Console Errors Warnings		
Generate System ACE or PFF file	PROM File Generation Target Xilinx PROM 8,197,280 Bits used File: fpga in Location	n: C:\Daten/

PROM File Formatter: Generate File...

You should see the following message in the main panel: generate succeeded.



iMPACT Save Project

In the folder corresponding to the path you chose as the output file location, you should find the fpga.mcs PROM file.