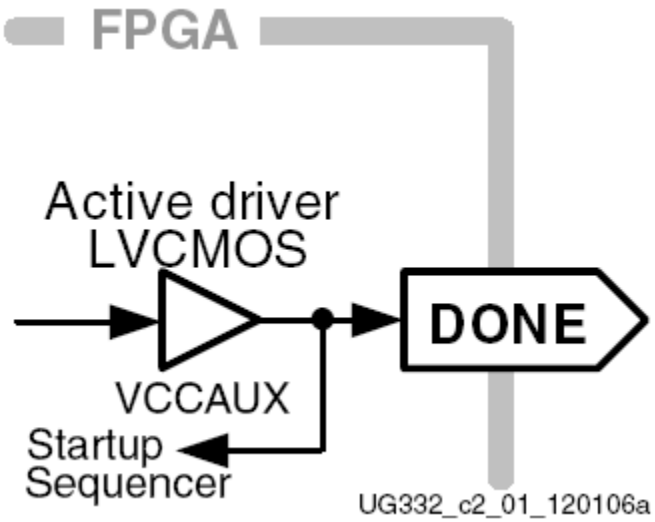
FPGA configuration process successfully completes (DONE PIN)

When the configuration process successfully completes, the FPGA either actively drives the DONE pin High (*DriveDone*) or allows the DONE pin to float High using either an internal or external pull-up resistor, controlled by the *DonePin* bitstream generator option. To have DONE LED D1 lit after successful FPGA configuration, DriveDone and DonePin bitstream generator options for the DONE pin have to be set to have DONE actively driving its line (see the figure and table below).

For the pull-up resistor value, see AR# 35002: Spartan-6 - Pull-up resistor value on INIT_B and DONE



DriveDone and DonePin set to have DONE actively driving its line.

DriveDone defines whether the DONE pin is an active driver or an open-drain output.
DonePin defines whether or not the DONE pin has an internal pull-up resistor.

bitstream generator (BitGen) option	Setting
DriveDone	Yes
DonePin	Pullnone

DriveDone and DonePin settings for having DONE actively driving its line.

See Xilinx UG332: Spartan-3 Generation Configuration User Guide (paragraph "DONE Pin") for additional information on these signals.
This options are set graphically in Xilinx ISE Software Project Navigator by selecting the following:
Generate Programming File > Process Properties > Startup Options > Drive Done Pin High > check the box
Generate Programming File > Process Properties > Configuration Options > Configuration Pin Done > float

Xilinx ISE Project Navigator option	setting
Drive Done Pin High	(checked)
Configuration Pin Done	Float

Xilinx ISE Project Navigator settings for having DONE actively driving its line.

Consult *ISE Help* about the Process Properties of the Generate Programming File process in the Processes pane for additional information on these properties.