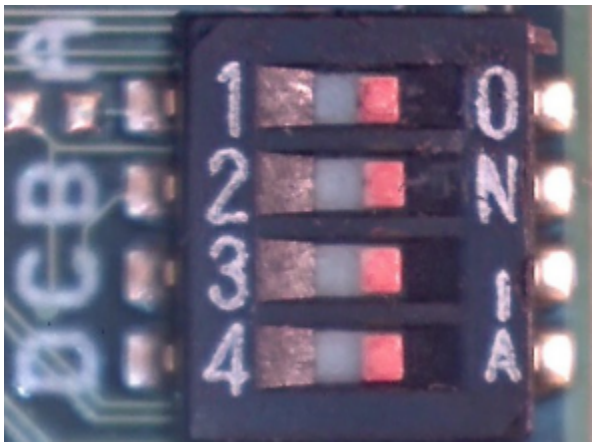
TE0630 Dip Switch S1B (Configuration)

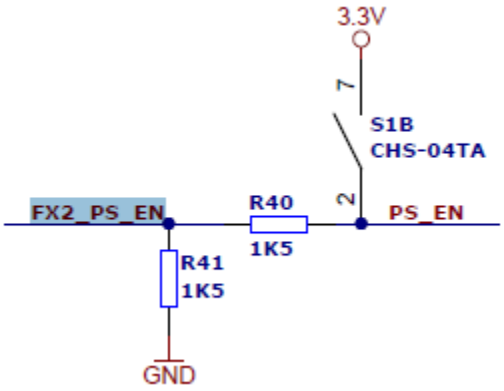
TE0630 is provided with a Dip switch S1B.
Dip switch S1B conditions the value of signal PS_EN.
In this way, S1B conditionally/unconditionally enables the power rails 1.2 V, 1.5 V and 2.5 V.

Please note the 4 switch labels are on one side and the <ON> label is on the opposite side.

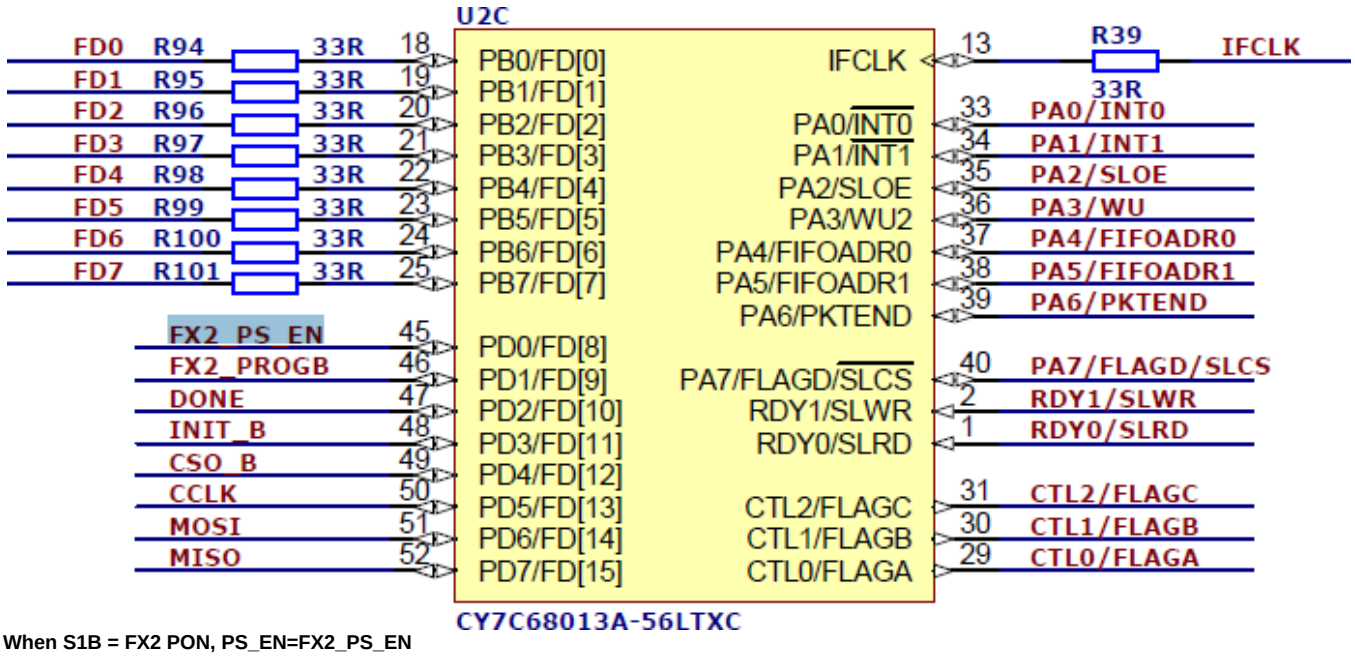
DIP slide switches S1[A:D] condition the value of some system signals as described in the table below.



Dip switch S1[A:D]. The switch S1B is the one with label 2 and B



Dip switch S1B schematic.



When S1B = FX2 PON, PS_EN=FX2_PS_EN

When S1B is turned **off** (**FX2 PON position**), the 1.2 V, 1.5 V and 2.5 V power rails are controlled by the USB (EZ-USB FX2LP USB FX2) microcontroller. At start-up, the USB microcontroller switches off the power rails 1.2 V, 1.5 V and 2.5 V and starts up the module in low-power mode. After enumeration, the USB microcontroller firmware enables (switches on) the power rails 1.2 V, 1.5 V and 2.5 V, if enough current is available from the USB bus.

When S1B is turned **on** (**PON position**), the power rails 1.2 V, 1.5 V and 2.5 V are always enabled (switched on).

S1B position	Default position	Effect on 1.2 V, 1.5 V and 2.5 V rails
FX2 PON (**off**)	✅	Power rails 1.2 V, 1.5 V and 2.5 V controlled by USB FX2 microcontroller (signal **FX2_PS_EN**) **PS_EN** = **FX2_PS_EN** = 1 or 0
PON (**on**)	❌	Power rails 1.2 V, 1.5 V and 2.5 V always enabled (**PS_EN** = 1) **PS_EN** **FX_PS_EN** = 1 or 0

Dip switch S1B settings overview (power rails 1.2 V, 1.5V and 2.5 V only).

Signal FX2_PS_EN

To command signal **FX2_PS_EN**, read the reference firmware code.
IOD = 0x03; // Enable PS_EN and disable PROG_B
OED = 0x03; // Configure PS_EN and PROG as outputs

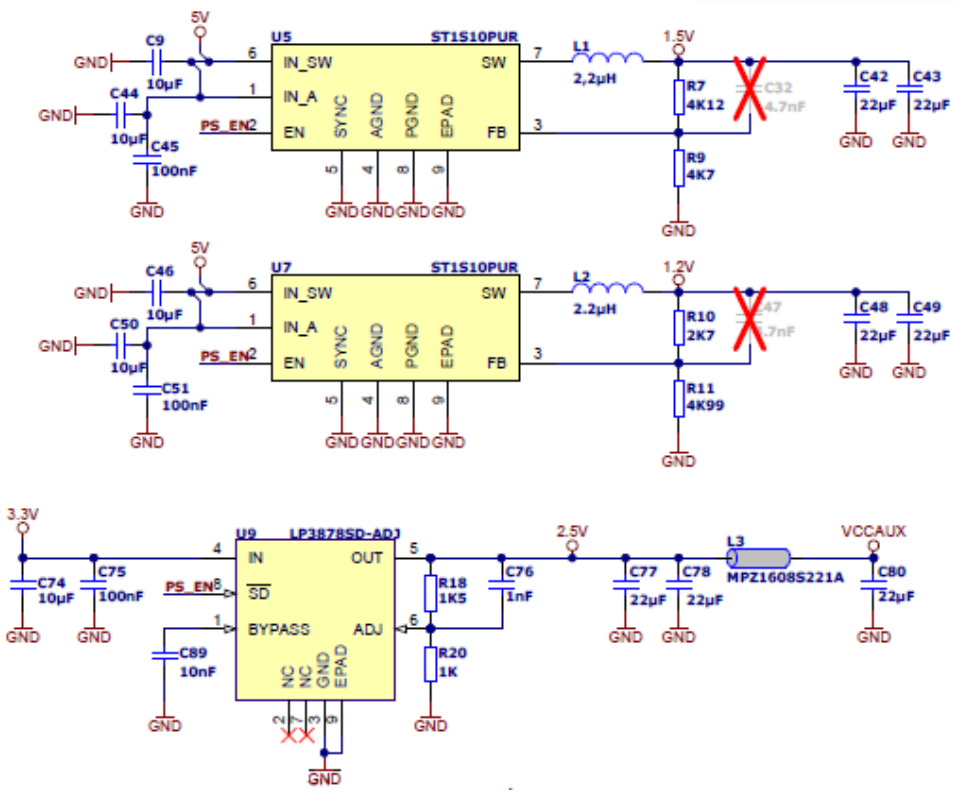
Table from **EZ-USB(R) Technical Reference Manual** (EZ-USB_TRM.pdf)

Port D Pin	Alternate Function	Alternate Function is Selected By...	Alternate Function is Described in...
PD[7:0]	FD[15:8]	IFCFG1 = 1 and any WORDWIIDE bit = 1	Slave FIFOs chapter 9 on page 99

Table from EZ-USB(R) Technical Reference Manual (EZ-USB_TRM.pdf).

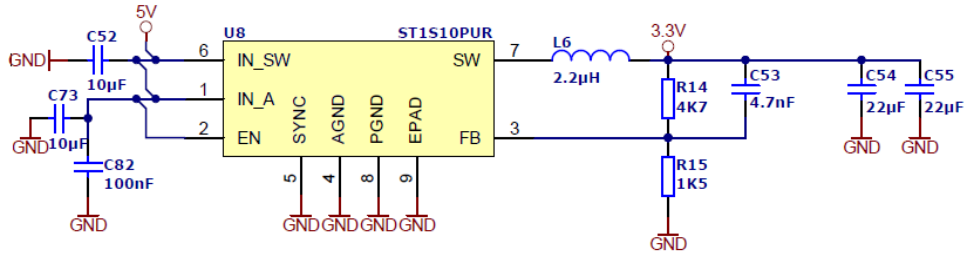
Signal PS_EN

- Signal PS_EN enables (1) or disables (0) power rails 1.2 V, 1.5 V and 2.5 V.



Power rails 1.2 V, 1.5 V and 2.5 V could be enabled/disabled by signal PS_EN.

- Power-rail 3.3V is not controlled by signal PS_EN and is unconditionally enabled.



Power rails 3.3V could not be enabled/disabled by signal PS_EN.

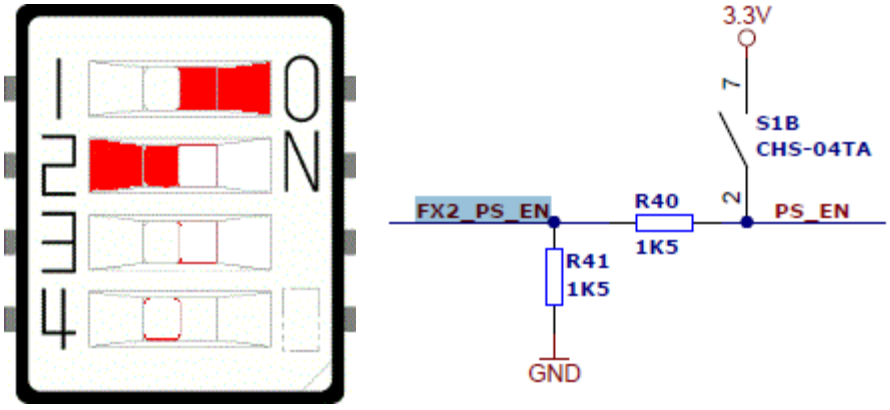
VCCIO assembly options

According to the corresponding assembly option, power rail VCCCIO0 (enabled by PS_EN and switch S1B) can depend or not on the power rail 2.5V.

See section "FPGA I/O banks power supply" here.

Dip Switch S1B = FX2 PON

When Dip switch **S1B is in the left position** (**= FX2 PON** : power rails conditionally on depending on signal FX2_PS_EN), signal **PS_EN is set to signal FX2_PS_EN** (**PS_EN = FX2_PS_EN**) driven by the EZ-USB FX2LP USB FX2 microcontroller under user control (IOD and OED of fw.c).

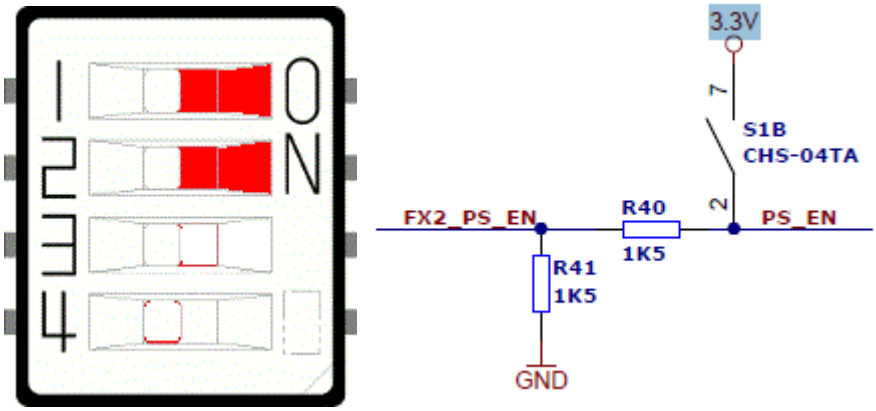


S1B on position FX2 PON (PS_EN = FX2_PS_EN = 1 or 0).

1. Dynamic **full power** operation (**PS_EN = 1**): when the EZ-USB FX2LP USB FX2 microcontroller sets signal **PS_EN = FX2_PS_EN = high**, power rails 1.2 V, 1.5 V and 2.5 V are enabled.
   This setting can be useful for .
2. Dynamic **low power** operation (**PS_EN = 0**): when the EZ-USB FX2LP USB FX2 microcontroller resets signal **PS_EN = FX2_PS_EN = low**, the following components are switched off:
   - FPGA core logic (1.2 V)
   - DDR SDRAM (2.5 V)
   - FPGA bank 1 (1.5 V)
   - VREF1 (0.75 V)
   - VCCCIO0 (2.5 V) FPGA bank 0 (if R102+R103- assembly)

Dip Switch S1B = PON

Full power operation (**PS_EN = 1**): when Dip switch S1B is in the right position (PON = power rails unconditionally on), signal PS_EN is set to power rail 3.3 V. Thus power rails 1.2 V, 1.5 V and 2.5 V are unconditionally enabled.



S1B on position PON (PS_EN FX2_PS_EN = x; PS_EN = high).

Summary table

The table below summarizes all switching options implied by Dip switch S1B and firmware signal FX2_PS_EN (under the standard assembly option).

power rail	S1B= PON (PS_EN = 1) (PS_EN FX2_PS_EN) (Full power)	S1B = FX2 PON and PS_EN = FX2_PS_EN = 1 (Dynamic full power)	S1B = FX2 PON and PS_EN = FX2_PS_EN = 0 (Dynamic low power)
1.2 V	**on**	**on**	**off**
1.5 V	**on**	**on**	**off**
2.5 V	**on**	**on**	**off**
VCCCIO0 (= 2.5 V) R102-R103+ assembly [(1)]	**on**	**on**	**off**
VCCCIO0 (= 3.3 V) R102+R103- assembly [(2)]	**on**	**on**	**on**

[(1)] R102 unpopulated / R103 populated

[(2)] R102 populated / R103 unpopulated

Dip switch S1B settings overview (1.2 V, 1.5 V , 2.5 V, VCCIO0).