TE0835 CPLD

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Overview

Firmware for RFSoC module CPLD with designator U31: LCMX02-640HC

Feature Summary

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Firmware Revision and supported PCB Revision

See Document Change History

Product Specification

Port Description

Name / opt. VHD Name	Direction	Pin	Bank Power	Description

PWR_STATUS	out	36	1.8 V_CPLD	Output for Status-LED (After successful configuration of FPGA is connected automatically with FPGA_IO0)
MODE0	out	35	1.8 V_CPLD	ZynqMP boot mode pin 0
PG_VCCRF	in	34	1.8 V_CPLD	Power Good input from PWR_PRE
SRST_B	out	33	1.8 V_CPLD	FPGA external system reset / currently_not_used
PROG_B	out	32	1.8 V_CPLD	FPGA reset PL configuration logic / currently_not_used
PG_GR2	in	31	1.8 V_CPLD	Power control input from PWR_PS and PWR_DDR
MIO28_UART1_TX	out	29	1.8 V_CPLD	UART Transmition pin / currently_not_used
MIO28_UART1_RX	in	28	1.8 V_CPLD	UART Receive pin / currently_not_used
FPGA_IO0	out	27	1.8 V_CPLD	FPGA GPIO / User LED
FPGA_IO1	inout	26	1.8 V_CPLD	FPGA GPIO / User dip switch interface
EN_PS_PL	out	14	3.3 V_CPLD	Power enable for PWR_CORE , PWR_PS and PWR_GT
EN_GR1	out	15	3.3 V_CPLD	Power enable for PWR_GT and PWR_PS
EN_RF_ADC	out	16	3.3 V_CPLD	Power enable for PWR_ADC
PG_RF_DAC	in	17	3.3 V_CPLD	Power control input from PWR_DAC
EN_VCCRF	out	18	3.3 V_CPLD	Power enable for PWR_PRE
EN_GR2	out	19	3.3 V_CPLD	Power enable for PWR_DDR , PWR_GT and PWR_PS
PG_PS_PL	in	20	3.3 V_CPLD	power control input from PWR_CORE , PWR_GT and PWR_PS
PG_GR1	in	21	3.3 V_CPLD	Power control input from PWR_GT and PWR_PS
PG_RF_ADC	in	23	3.3 V_CPLD	Power control input from PWR_ADC
EN_RF_DAC	out	24	3.3 V_CPLD	Power enable for PWR_DAC
MODE2	out	2	1.8 V_CPLD	ZynqMP boot mode pin 2
MODE1	out	3	1.8 V_CPLD	ZynqMP boot mode pin 1
POR_B	out	4	1.8 V_CPLD	Power-On reset signal
MODE3	out	5	1.8 V_CPLD	ZynqMP boot mode pin 3
INIT_B	in	7	1.8 V_CPLD	FPGA PL initialization activity and configuration error signal / currently_not_used
F_TDI	out	8	1.8 V_CPLD	JTAG ZynqMP

F_TMS	out	9	1.8 V_CPLD	JTAG ZynqMP
F_TCK	out	10	1.8 V_CPLD	JTAG ZynqMP
F_TDO	in	11	1.8 V_CPLD	JTAG ZynqMP
DONE	in	12	1.8 V_CPLD	FPGA PL configuration done indicator
JTAG_TDO	out	48	3.3 V_CPLD	JTAG_B2B
JTAG_TDI	in	47	3.3 V_CPLD	JTAG_B2B
JTAG_TCK	in	45	3.3 V_CPLD	JTAG_B2B
JTAG_TMS	in	44	3.3 V_CPLD	JTAG_B2B
CPLD_IO0	in	43	3.3 V_CPLD	BOOT Mode input pin 0
CPLD_IO1	in	42	3.3 V_CPLD	BOOT Mode input pin 1
CPLD_JTAGEN	in	41	3.3 V_CPLD	Enable JTAG access to CPLD for Firmware update (zero: JTAG routed to module, one: CPLD access)
CPLD_IO2	in	40	3.3 V_CPLD	CPLD IO to B2B / Used as dip switch interface on the carrier board (After successful configuration of FPGA is connected automatically with FPGA_IO1)
CPLD_IO3	out	38	3.3 V_CPLD	CPLD IO to B2B/ Used as power good, can be used to enable carrier periphery power
RESETN	in	37	3.3 V_CPLD	Reset pin (Active low)

Functional Description

JTAG

JTAG signals routed directly through the CPLD to FPGA. Access between CPLD and FPGA can be multiplexed via JTAGEN (logical one for CPLD, logical zero for FPGA) on B2B. In the carrier board TEB0835 can be activated this pin with S1-4 dip switch.

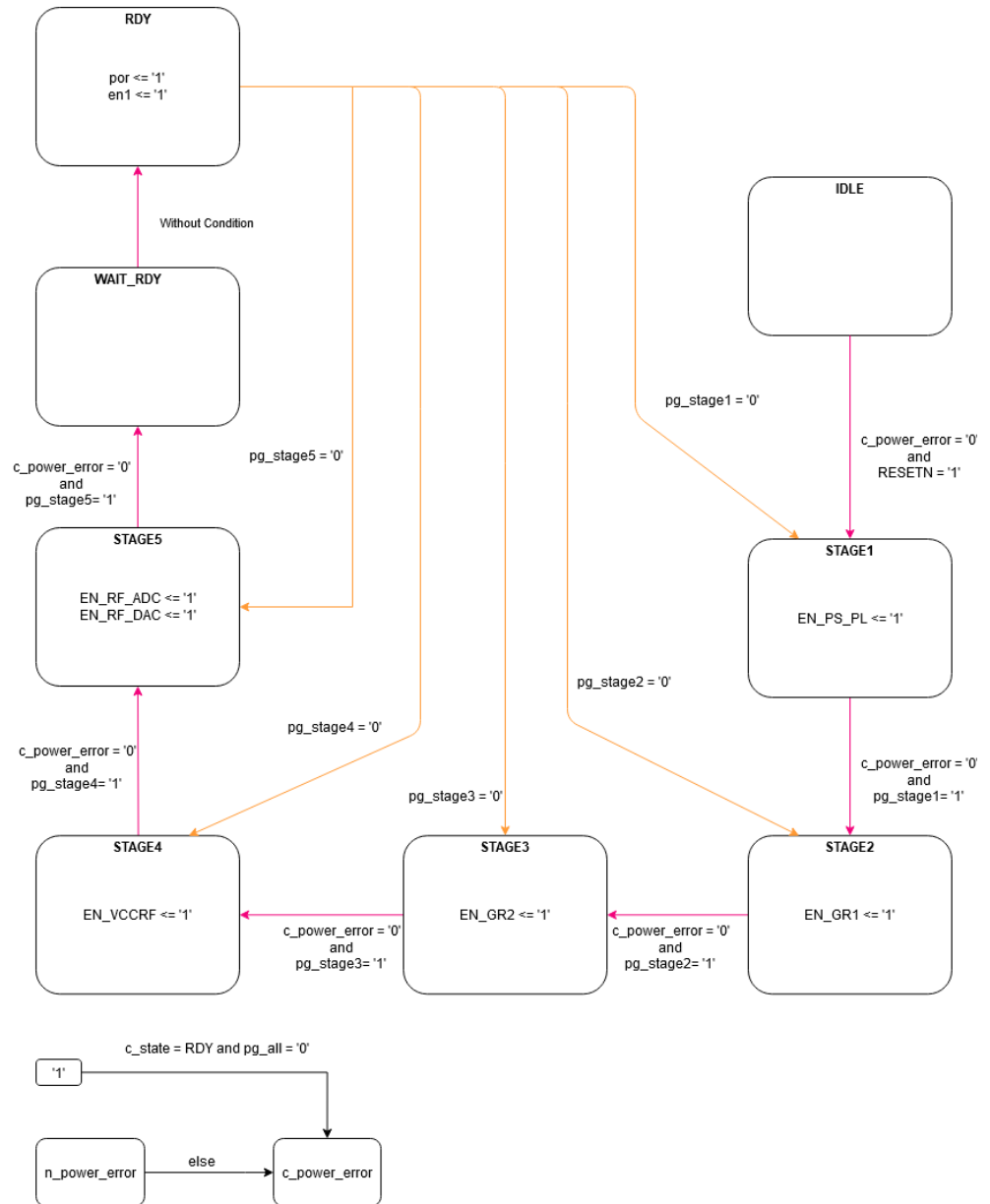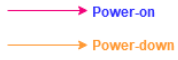| CPLD_JTAGEN (B2B J1-30)	S1-4 on TEB0835 Carrier Board	Description
0	OFF	FPGA access
1	ON	CPLD access

Power

In this module the CPLD is responsible for controlling the power of the module. There are different power regulators or DC/DC converters whose outputs can be controlled by an enable signal. At the same time the outputs can also be monitored by power-good signals.

Enable Signal	Power Good Signal	Schematic page	Net	Domain	Regulator/ DC-DC Converter	in/out Voltage

EN_PS_PL	PG_PS_PL	PWR_CORE	VCCINT, VCINT_IO, VCCBRAM	PL	LTM4662EY	5V/0.835V
		PWR_PS	PSINTLP/PSINTFP,PSINTFP_DDR	PS_LP /PS_FP	LTM4644EY	5V/0.85V
		PWR_GT	MGTAVCC	GTH	TPS82085	5V/0.9V
EN_GR1	PG_GR1	PWR_PS	PSAUX,PSADC,PSIO/VCCAUX,VCCAUX_IO /PS_DDR_PLL	PS_LP/PL /PS_FP	TPS82085	5V/1.8V
		PWR_GT	PSMGTRAVCC/MGTVCCAUX	PS_FP/GTH	EP53A7LQI	5V/0.85V
		PWR_GT	PSPLL/MGTAVTT	PS_LP/GTH	EN6347QI	5V/1.2V
EN_GR2	PG_GR2	PWR_PS	VCC_B88_HD	PS_LP	TPS82085	5V/3.3V
		PWR_GT	PS_MGTRAVTT	PS_FP	EP53A7HQI	5V/1.8V
		PWR_DDR	DDR_2V5	DDR	TPS82085	5V/2.5V
		PWR_DDR	DDR_1V2	DDR	TPS82085	5V/1.2V
EN_VCCRF	PG_VCCRF	PWR_PRE	VCCINT_AMS, APRE_1V15, APRE_3V3	ADC and DAC	LTM4644EY	5V/0.8534V,1.15 V,3.3V
EN_RF_ADC	PG_RF_ADC	PWR_ADC	ADC_AVCC	ADC	TPS74401	1.15V/0.925V
		PWR_ADC	ADC_AVCCAUX	ADC	TPS74401	3.3V/1.8V
EN_RF_DAC	PG_RF_DAC	PWR_DAC	DAC_AVCC	DAC	TPS74801	5V/0.925V
		PWR_DAC	DAC_AVCCAUX	DAC	TPS74801	5V/1.8V
		PWR_DAC	DAC_AVTT	DAC	TPS74801	5V/2.5V

Power-on Sequencing

According to the Xilinx instructions the power regulator or DC-DC converter must be switched on or off in a certain order. This is called power-on or power-off sequencing.To implement power-on sequencing correctly, a state machine must be running there. In the following you can see the State Machine Diagram.

Power-on
Power-down

RDY
por <= '1'
en1 <= '1'

IDLE

WAIT_RDY

Without Condition

c_power_error = '0'
and
pg_stage5= '1'

pg_stage5 = '0'

pg_stage1 = '0'

c_power_error = '0'
and
RESETN = '1'

STAGE5
EN_RF_ADC <= '1'
EN_RF_DAC <= '1'

STAGE1
EN_PS_PL <= '1'

c_power_error = '0'
and
pg_stage4= '1'

pg_stage4 = '0'

pg_stage2 = '0'

c_power_error = '0'
and
pg_stage1= '1'

pg_stage3 = '0'

STAGE4
EN_VCCRF <= '1'

STAGE3
EN_GR2 <= '1'

STAGE2
EN_GR1 <= '1'

c_power_error = '0'
and
pg_stage3= '1'

c_power_error = '0'
and
pg_stage2= '1'

c_state = RDY and pg_all = '0'

'1'

n_power_error   else   c_power_error

Stage	Control	Voltage Domains	Signal Monitoring to change stage
IDLE	---	---	RESETN
STAGE1	EN_PS_PL enabled (High)	0.853V, 0.85V, 0.9V	PG_PS_PL
STAGE2	EN_GR1 enabled (High)	1.8V, 0.85V, 1.2V	PG_GR1
STAGE3	EN_GR2 enabled (High)	3.3V, 1.8V	PG_GR2
STAGE4	EN_VCCRF enabled (High)	0.8534V, 1.158V, 3.3V	PG_VCCRF

STAGE5	EN_RF_ADC enabled (High)	0.925V, 1.8V	PG_RF_ADC
	EN_RF_DAC enabled (High)	0.925V, 1.8V, 2.5V	PG_RF_DAC
WAIT_RDY	---	---	---
RDY	por enabled (High)	---	pg_all
	en1 enabled (High) if DONE is High.		

- pg_all <= PG_PS_PL & PG_GR1 & PG_GR2 & PG_VCCRF & PG_RF_ADC & PG_RF_DAC
- If por is high then POR_B (power-on reset signal) will be deactivated.

LED

States	Blink Sequence	Comment
IDLE	ooooooooooo ooooooooo*	Power Sequencing can not start. RESETN is active.
Stage 1	ooooooooooo oooooo*o*	The correct voltage in one of the following nets are failed: VCCINT, VCINT_IO, VCCBRAM, PSINTLP, PSINTFP, PSINTFP_DDR, MGTAVCC
Stage 2	ooooooooooo oooo*o*o*	The correct voltage in one of the following nets are failed: PSAUX, PSADC, PSIO, VCCAUX, VCCAUX_IO, PS_DDR_PLL, PSMGTRAVCC, MGTVCCAUX, PSPLL, MGTAVTT
Stage 3	ooooooooooo oo*o*o*o*	The correct voltage in one of the following nets are failed: VCC_B88_HD, PS_MGTRAVTT, DDR_2V5 , DDR_1V2
Stage 4	ooooooooooo* o*o*o*o*	The correct voltage in one of the following nets are failed: VCCINT_AMS, APRE_1V15, APRE_3V3
Stage 5	oooooooooo*o* o*o*o*o*	The correct voltage in one of the following nets are failed: ADC_AVCC, ADC_AVCCAUX, DAC_AVCC, DAC_AVCCAUX, DAC_AVTT
WAIT_RDY / RDY and DONE='0'	ooooooo*o*o* o*o*o*o*	Power is ok. But the FPGA is not yet configured.
pg_all = '0'	ooooo*o*o*o*o *o*o*o*	An unknown error has occurred. The power supply must be switched off.
USR (RDY and DONE='1')	User defined	Power is ok and the FPGA is configured successfully. LED can be controlled by user, when Power is OK and FPGA part is programmed (DONE signal is high)

- The period for erery blink (*o) is 0.5sec.

User IO

- FPGA_IO1 (AE16 of RFSoC) is connected with CPLD_IO2 (S1-3 Dip switch on the carrier board) when the FPGA is programmed correctly otherweise this pin is high impedance. After configuration of the FPGA can user use this pin as input.
- FPGA_IO0 (AE18 of RFSOC) is connected with LED on the RFSoC module (D1) if the FPGA is programmed completely otherweise this LED (D1) blinks according to the state of the power-on sequencing. After configuration of the FPGA can be controlled this LED (D1) by user.

If the FPGA correctly programmed (DONE signal is high) and the power-on sequencing state is RDY then the User IOs can be shown in the following table:

Function	Interface	Schematic	FPGA Pin	Note
USER signal	B2B (J1-32)	FPGA_IO1	AE16	source by TEB0835 Dip Switch S1-3, in case FPGA is programmed
LED (D1)	--	FPGA_IO0	AE18	controls LED, in case FPGA is programmed

Boot Mode

Boot Modes can be selected via B2B Pin Mode.

B2B Pin J1-28 (CPLD IO1)	B2B Pin J1-26 (CPLD IO0)	Boot Mode
0	0	Boot from PS JTAG
0	1	Boot from QSPI
1	1	Boot from SD Card

Appx. A: Change History and Legal Notices

Revision Changes

- REV00 to REV01
    - transfer verilog to vhdl
    - power stagemachine, add power down cyclus on error state
    - bugfix: Power Good(CPLD_IO3) depends now on module power sequencing
    - LED status changed
    - LED controllable by USR after power up
    - CPLD_IO2 connected to FPGA IO (can be controlled by user)
    - constrains and buffer changes for JTAG

Document Change History

To get content of older revision got to "Change History" of this page and select older document revision number.

Date	Document Revision	CPLD Firmware Revision	Supported PCB Revision	Authors	Description
		REV01	REV02, REV01	**Error rendering macro 'page-info'** Ambiguous method overloading for method jdk. proxy241.$ Proxy3496 #hasConte	• REV01 release (firmware release 2020-10-27)

Error rendering macro 'page-info'

Ambiguous method overloading for method jdk.proxy241.$Proxy3496#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]

					user.User, class java. lang. String, class com. atlassian. confluence .core. ContentEn tityObject]
2020-08-18	v.4	REV00	REV01	Ivan Girshchenko / Mohsen Chamanbaz	• REV00 release (firmware release 2019-12-18)
	All				**Error rendering macro 'page-info'** Ambiguou s method overloadin g for method jdk. proxy241.$ Proxy3496 #hasConte ntLevelPer mission. Cannot resolve which method to invoke for

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| | | | | | .core.

ContentEn

tityObject] | |

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