

TE0808 SK Demo1

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Overview

Linux with basic periphery of TE0808 Starterkit (TEBF0808 Carrier).

Refer to <http://trenz.org/te0808-info> for the current online version of this manual and other available documentation.

Key Features

- Vitis/Vivado 2019.2
- petalinux
- Linux Debian 9 (Stretch) or Linux Ubuntu 18.04 (Bionic Beaver)
- DisplayPort
- TEBF0808
- USB
- ETH (use EEPROM MAC)
- MAC from EEPROM
- PCIe
- SATA
- SD
- I2C
- RGPIIO
- DP
- user LED access
- Modified FSBL for Si5338 programming
- Special FSBL for QSPI Programming

Revision History

Date	Vivado	Project Built	Authors	Description
2020-05-11	2019.2	TE0808-SK_DEMO1_noprebuilt-vivado_2019.2-build_11_20200511131530.zip TE0808-SK_DEMO1-vivado_2019.2-build_11_20200511131516.zip	Mohsen Chamanbaz	<ul style="list-style-type: none">• initial release

Design Revision History

Release Notes and Know Issues

Issues	Description	Workaround/Solution	To be fixed version
No known issues	---	---	---

Known Issues

Requirements

Software

Software	Version	Note
Vitis	2019.2	needed, Vivado is included into Vitis installation
PetaLinux	2019.2	needed
SD Card Formatter		format SD Card
Win32 DiskImager		burn generated image on SD
SI ClockBuilder Pro	---	optional

Software

Hardware

Basic description of TE Board Part Files is available on [TE Board Part Files](#).

Complete List is available on <design name>/board_files/*_board_files.csv

Design supports following modules:

Module Model	Board Part Short Name	PCB Revision Support	DDR	QSPI Flash	EMMC	Others	Notes
TE0808-ES1	es1_2gb	REV03 REV02	2GB	64MB	NA	NA	Not longer supported by vivado
TE0808-ES2	es2_2gb	REV04 REV03	2GB	64MB	NA	NA	Not longer supported by vivado
TE0808-2ES2	2es2_2gb	REV04 REV03	2GB	64MB	NA	NA	Not longer supported by vivado
TE0808-04-09EG-1EA	9eg_1e_2gb	REV04	2GB	64MB	NA	NA	
TE0808-04-09EG-1EB	9eg_1e_4gb	REV04	4GB	64MB	NA	NA	
TE0808-04-09EG-1ED	9eg_1e_4gb	REV04	4GB	64MB	NA	1 mm connectors	
TE0808-04-09EG-2IB	9eg_2i_4gb	REV04	4GB	64MB	NA	NA	
TE0808-04-15EG-1EB	15eg_1e_4gb	REV04	4GB	64MB	NA	NA	
TE0808-04-09EG-1EE	9eg_1e_4gb	REV04	4GB	128MB	NA	NA	
TE0808-04-09EG-1EL	9eg_1e_4gb	REV04	4GB	128MB	NA	1 mm connectors	
TE0808-04-09EG-2IE	9eg_2i_4gb	REV04	4GB	128MB	NA	NA	
TE0808-04-15EG-1EE	15eg_1e_4gb	REV04	4GB	128MB	NA	NA	
TE0808-04-06EG-1EE	6eg_1e_4gb	REV04	4GB	128MB	NA	NA	
TE0808-04-06EG-1E3	6eg_1e_4gb	REV04	4GB	128MB	NA	1 mm connectors	
TE0808-04-6GI21-L	6eg_2i_4gb	REV04	4GB	128MB	NA	1 mm connectors	
TE0808-04-6GI21-A	6eg_2i_4gb	REV04	4GB	128MB	NA	NA	
TE0808-04-6BI21-A	6eg_1i_4gb	REV04	4GB	128MB	NA	NA	
TE0808-04-9GI21-A	9eg_2i_4gb	REV04	4GB	128MB	NA	NA	
TE0808-04-9BE21-A	9eg_1e_4gb	REV04	4GB	128MB	NA	NA	
TE0808-04-6BE21-L	6eg_1e_4gb	REV04	4GB	128MB	NA	1 mm connectors	
TE0808-04-6BE21-A	6eg_1e_4gb	REV04	4GB	128MB	NA	NA	
TE0808-04-9BE21-L	9eg_1e_4gb	REV04	4GB	128MB	NA	1 mm connectors	
TE0808-04-BBE21-A	15eg_1e_4gb	REV04	4GB	128MB	NA	NA	
TE0808-04-6BI21-X	6eg_1i_4gb	REV04	4GB	128MB	NA	NA	U41 replaced with schottky diodes

Hardware Modules

Note: Design contains also Board Part Files for TE0808 only configuration, this board part files are not used for this reference design.

Design supports following carriers:

Carrier Model	Notes
TEBF0808	Used as reference carrier. Important: CPLD Firmware REV07 or newer is recommended

Hardware Carrier

Additional HW Requirements:

Additional Hardware	Notes
Cooler	It's recommended to use cooler on ZynqMP device

USB Cable	Connect to USB2 or better USB3 Hub for proper power supply over USB
DP Monitor	Optional HW Not all monitors are supported, also adapter to other standards can make trouble. Design was tested with DELL U2412M
Micro USB to USB A Adapter	Adapter for USB Hub
USB HUB	To connect Mouse and Keyboard simultaneously
USB Keyboard	need for Ubuntu/Debian GUI
USB Mouse	need for Ubuntu/Debian GUI
DP Cable	--
Sata Disk	Optional HW
SATA Cable	Optional HW
PCIe Card	Optional HW
ETH Cable	Optional HW Ethernet works with DHCP, but can be setup also manually
SD Card	16GB

Additional Hardware

Content

For general structure and of the reference design, see [Project Delivery - AMD devices](#)

Design Sources

Type	Location	Notes
Vivado	<design name>/block_design <design name>/constraints <design name>/ip_lib	Vivado Project will be generated by TE Scripts
Vitis	<design name>/sw_lib	Additional Software Template for Vitis and apps_list.csv with settings automatically for Vitis app generation
PetaLinux	<design name>/os/petalinux	PetaLinux template with current configuration

Design sources

Additional Sources

Type	Location	Notes
SI5345	<design name>/misc/SI5345	SI5345 Project with current PLL Configuration

Additional design sources

Prebuilt

File	File-Extension	Description
BIF-File	*.bif	File with description to generate Bin-File

BIN-File	*.bin	Flash Configuration File with Boot-Image (Zynq-FPGAs)
BIT-File	*.bit	FPGA (PL Part) Configuration File
DebugProbes-File	*.ltx	Definition File for Vivado/Vivado Labtools Debugging Interface
Diverse Reports	---	Report files in different formats
Hardware-Platform-Specification-Files	*.xsa	Exported Vivado Hardware Specification for Vitis and PetaLinux
LabTools Project-File	*.lpr	Vivado Labtools Project File
OS-Image	*.ub	Image with Linux Kernel (On Petalinux optional with Devicetree and RAM-Disk)
Image	---	Generic Linux kernel binary image file
Software-Application-File	*.elf	Software Application for Zynq or MicroBlaze Processor Systems
Device Tree Blob File	*.dtb	Contains a Device Tree Blob

Prebuilt files (only on ZIP with prebuilt content)

Download

Reference Design is only usable with the specified Vivado/SDK/PetaLinux/SDx version. Do never use different Versions of Xilinx Software for the same Project.

Reference Design is available on:

- [TE0808 "SK DEMO1" Reference Design](#)

Design Flow



Reference Design is available with and without prebuilt files. It's recommended to use TE prebuilt files for first lunch.

Trenz Electronic provides a tcl based built environment based on Xilinx Design Flow.

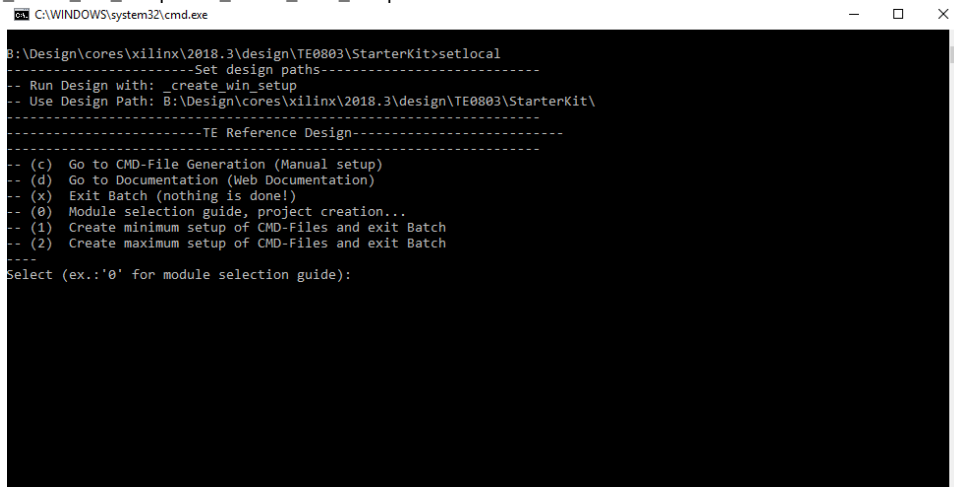
See also:

- [AMD Development Tools#XilinxSoftware-BasicUserGuides](#)
- [Vivado Projects - TE Reference Design](#)
- [Project Delivery](#).

The Trenz Electronic FPGA Reference Designs are TCL-script based project. Command files for execution will be generated with "_create_win_setup.cmd" on Windows OS and "_create_linux_setup.sh" on Linux OS.

TE Scripts are only needed to generate the vivado project, all other additional steps are optional and can also executed by Xilinx Vivado/SDK GUI. For currently Scripts limitations on Win and Linux OS see: [Project Delivery Currently limitations of functionality](#)

1. `_create_win_setup.cmd/_create_linux_setup.sh` and follow instructions on shell:



2. Press 0 and enter to start "Module Selection Guide"
3. (optional Win OS) Generate Virtual Drive or use short directory for the reference design (for example x:\<design name>)
4. Create Project (follow instruction of the product selection guide), settings file will be configured automatically during this process)
 - a. (optional for manual changes) Select correct device and Xilinx install path on "design_basic_settings.cmd" and create Vivado project with "vivado_create_project_gui mode.cmd"
Note: Select correct one, see also [TE Board Part Files](#)
 - i. **Important:** Use Board Part Files, which ends with *_tebf0808
5. Create XSA and export to prebuilt folder
 - a. Run on Vivado TCL: `TE::hw_build_design -export_prebuilt`
Note: Script generate design and export files into \prebuilt\hardware\<short dir>. Use GUI is the same, except file export to prebuilt folder
6. Create Linux (bl31.elf, uboot.elf, Image and system.dtb) with exported XSA
 - a. XSA is exported to "prebuilt\hardware\<short name>"
Note: HW Export from Vivado GUI create another path as default workspace.
Create Linux images on VM, see [PetaLinux KICKstart](#)
 - i. Use TE Template from /os/petalinux/
 - ii. Execute the script file for Debian/Ubuntu
7. Add Linux files (bl31.elf, uboot.elf, Image and system.dtb) to prebuilt folder
 - a. "prebuilt\os\petalinux\<ddr size>" or "prebuilt\os\petalinux\<short name>"
8. Generate Programming Files with Vitis
 - a. Run on Vivado TCL: `TE::sw_run_vitis -all`
Note: Scripts generate applications and bootable files, which are defined in "sw_lib\apps_list.csv"
 - b. (alternative) Start SDK with Vivado GUI or start with TE Scripts on Vivado TCL: `TE::sw_run_vitis`
Note: TCL scripts generate also platform project, this must be done manually in case GUI is used. See [Vitis](#)
9. Preparing SD card for SD Filesystem and hard disk for HD Filesystem See Programming section

Launch

For basic board setup, LEDs... see: [TEBF0808 Getting Started](#)

Programming



Check Module and Carrier TRMs for proper HW configuration before you try any design.

Xilinx documentation for programming and debugging: [Vivado/SDK/SDSoC-Xilinx Software Programming and Debugging](#)

Get prebuilt boot binaries

1. `_create_win_setup.cmd/_create_linux_setup.sh` and follow instructions on shell

2. Press 0 and enter to start "Module Selection Guide"
 - a. Select assembly version
 - b. Validate selection
 - c. Select Create and open delivery binary folder

Note: Folder (<project folder>/_binaries_<Artikel Name>) with subfolder (boot_<app name>) for different applications will be generated

QSPI

Not used in this example.

SD

1. Format the SD Card with SD Card Formatter or other tool
2. Write the Debian image or Ubuntu image file on SD Card with Win32DiskImager
3. select the device tree depending on your ROOTFS location:
 - a. system_sd.dtb : This file ist used , if the root file system is located on SD card.
 - b. system_harddisk.dtb : This file ist used , if the root file system is located on hard disk.
 - c. Note: To use one of the DTB files, this file must be renamed to system.dtb
4. Rename selected device tree to system.dtb (for Hard Disk usage, see also "Hard Disk (optional)")
5. Copy Petalinux Image (not use image.ub), system.dtb and Boot.bin files on SD-Card.
 - use files from (<project folder>/_binaries_<Articel Name>)/boot_linux from generated binary folder, see: [Get prebuilt boot binaries](#)
 - or use prebuilt file location, see <design_name>/prebuilt/readme_file_location.txt
6. Set Boot Mode to SD-Boot.
 - Depends on Carrier, see carrier TRM.
7. Insert SD-Card in SD-Slot.

JTAG

Not used on this Example.

Usage

1. Prepare HW like described on section [TE0808 StarterKit#Programming](#)
2. Connect UART USB (JTAG XMOD)
3. Select SD Card as Boot Mode (or QSPI - depending on step 1)

Note: See TRM of the Carrier, which is used.
4. (Optional) Insert PCIe Card (detection depends on Linux driver. Only some basic drivers are installed)
5. (Optional) Connect Sata Disc
6. (Optional) Connect DisplayPort Monitor (List of usable Monitors: <https://www.xilinx.com/support/answers/68671.html>)
7. (Optional) Connect Network Cable
8. Power On PCB

Note: 1. ZynqMP Boot ROM loads PMU Firmware and FSBL from SD into OCM, 2. FSBL loads ATF(bl31.elf) and U-boot from SD/QSPI into DDR, 3. U-boot load Linux from SD into DDR.

Linux

1. Open Serial Console (e.g. putty)
 - a. Speed: 115200
 - b. COM Port: Win OS, see device manager, Linux OS see `dmesg |grep tty` (UART is *USB1)
2. Linux Console:

Note: Wait until Linux boot finished For Linux Login use:

 - a. User Name: root
 - b. Password: root
3. You can use Linux shell now.
4. Debian Desktop
 - a. Use connected mouse + keyboard for interaction with GUI
 - b. Start the GUI with the command : `startx`
 - c. Web Browser Dillo open console and type `dillo` or use browser
 - d. open console and start video or audio with `"mplayer <video or audio file>"`
5. Ubuntu Desktop
 - a. Use connected mouse + keyboard for interaction with GUI
 - b. Start the GUI with the command : `startx`

- c. Web Browser Mozilla firefox can be used.
- d. Audio or Video file can also be performed directly in GUI

Hard Disk (optional)

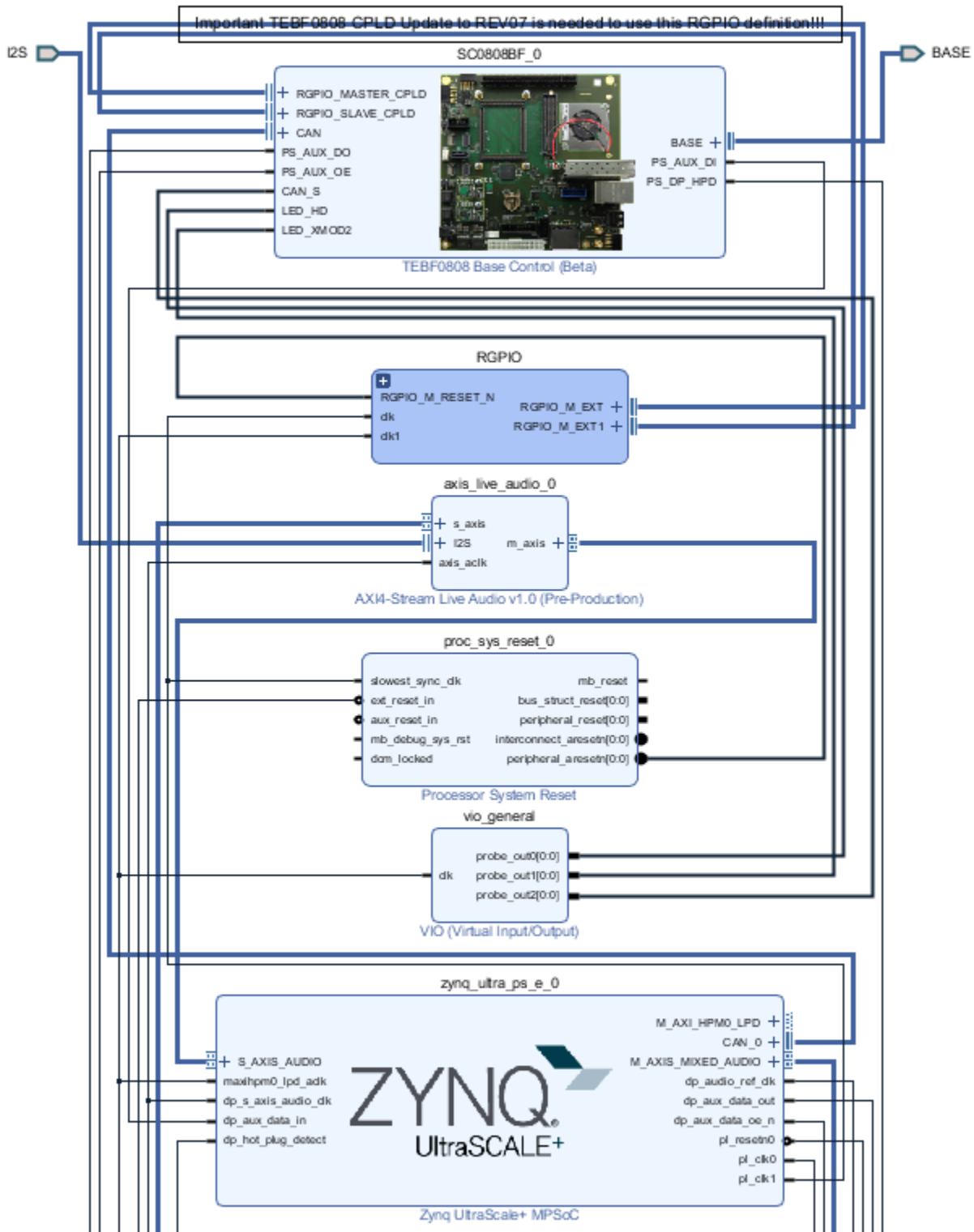
To locate root file system on Hard disk:

1. Plug in SD Card that you have prepared with root file system. It will automatically in BOOT directory two DTB file generated
2. Plug in Hard Disk in SATA port on the carrier board
3. Format the hard disk by the following command:
 - a. `mkfs.ext4 /dev/sda`
4. Edit the fstab file in directory /etc/ to mount hard disk by the following commands:
 - a. `mkdir /media/harddisk`
 - b. `nano /etc/fstab`
 - c. Add this line to the fstab file and save it : `/dev/sda /media/harddisk/ defaults 0 3`
 - d. Reboot
5. Copy entire root file system in directory ROOTFS from SD card to hard disk by the following commands:
 - a. `cd /media/ROOTFS`
 - b. `cp -r . /media/harddisk`
6. Edit the fstab file in directory /media/harddisk/etc/ by the following commands and save it:
 - a. `nano /media/harddisk/etc/fstab`
 - b. Edit this line to the fstab file : `/dev/sda /media/harddisk/ defaults 0 1`
 - c. Comment this line: `#/dev/mmcblk1p2 /media/ROOTFS defaults 0 1`
7. Shutdown the system
8. Format the SD card
9. Rename the Device Tree Blob file system_harddisk.dtb to system.dtb
10. Copy the following files to SD Card:
 - a. Image
 - b. BOOT.bin
 - c. system.dtb
11. Plug in the SD Card and turn on the system

Vivado Hardware Manager

System Design - Vivado

Block Design





Block Design

PS Interfaces

Activated interfaces:

Type	Note
DDR	
QSPI	MIO
SD0	MIO
SD1	MIO
I2C0	MIO
UART0	MIO
GPIO0	MIO
SWDT0..1	
TTC0..3	
GEM3	MIO
USB0	MIO/GTP
SATA	GTP
DisplayPort	EMIO/GTP
PCIe	MIO/GTP
CAN0	EMIO
PJTAG0	MIO

PS Interfaces

Constrains

Basic module constrains

_i_bitgen.xdc
<pre>set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design] set_property BITSTREAM.CONFIG.UNUSEDPIN PULLNONE [current_design]</pre>
_i_io.xdc

```

#System Controller IP
#LED_HD SC0 J3:31
#LED_XMOD SC17 J3:48
#CAN RX SC19 J3:52 B47_L2_P in
#CAN TX SC18 J3:50 B47_L2_N out
#CAN S SC16 J3:46 B47_L3_N out
set_property PACKAGE_PIN J14 [get_ports BASE_sc0]
set_property PACKAGE_PIN G13 [get_ports BASE_sc5]
set_property PACKAGE_PIN J15 [get_ports BASE_sc6]
set_property PACKAGE_PIN K15 [get_ports BASE_sc7]
set_property PACKAGE_PIN A15 [get_ports BASE_sc10_io]
set_property PACKAGE_PIN B15 [get_ports BASE_sc11]
set_property PACKAGE_PIN C13 [get_ports BASE_sc12]
set_property PACKAGE_PIN C14 [get_ports BASE_sc13]
set_property PACKAGE_PIN E13 [get_ports BASE_sc14]
set_property PACKAGE_PIN E14 [get_ports BASE_sc15]
set_property PACKAGE_PIN A13 [get_ports BASE_sc16]
set_property PACKAGE_PIN B13 [get_ports BASE_sc17]
set_property PACKAGE_PIN A14 [get_ports BASE_sc18]
set_property PACKAGE_PIN B14 [get_ports BASE_sc19]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc0]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc5]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc6]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc7]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc10_io]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc11]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc12]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc13]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc14]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc15]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc16]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc17]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc18]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc19]

# PLL
#set_property PACKAGE_PIN AH6 [get_ports {si570_clk_p[0]}]
#set_property IOSTANDARD LVDS [get_ports {si570_clk_p[0]}]
#set_property IOSTANDARD LVDS [get_ports {si570_clk_n[0]}]
# Clocks
#set_property PACKAGE_PIN J8 [get_ports {B229_CLK1_clk_p[0]}]
#set_property PACKAGE_PIN F25 [get_ports {B128_CLK0_clk_p[0]}]
# SFP
#set_property PACKAGE_PIN G8 [get_ports {B230_CLK0_clk_p}]
# B230_RX3_P
#set_property PACKAGE_PIN A4 [get_ports {SFP1_rxp}]
# B230_TX3_P
#set_property PACKAGE_PIN A8 [get_ports {SFP1_txp}]
# B230_RX2_P
#set_property PACKAGE_PIN B2 [get_ports {SFP2_rxp}]
# B230_TX2_P
#set_property PACKAGE_PIN B6 [get_ports {SFP2_txp}]

# Audio Codec
#LRCLK J3:49 B47_L9_N
#BCLK J3:51 B47_L9_P
#DAC_SDATA J3:53 B47_L7_N
#ADC_SDATA J3:55 B47_L7_P
set_property PACKAGE_PIN G14 [get_ports I2S_lrclk ]

```

```
set_property PACKAGE_PIN G15 [get_ports I2S_bclk ]
set_property PACKAGE_PIN E15 [get_ports I2S_sdin ]
set_property PACKAGE_PIN F15 [get_ports I2S_sdout ]
set_property IOSTANDARD LVCMOS18 [get_ports I2S_lrclk ]
set_property IOSTANDARD LVCMOS18 [get_ports I2S_bclk ]
set_property IOSTANDARD LVCMOS18 [get_ports I2S_sdin ]
set_property IOSTANDARD LVCMOS18 [get_ports I2S_sdout ]
```

Software Design - Vitis

For SDK project creation, follow instructions from:

[Vitis](#)

Application

SDK template in ./sw_lib/sw_apps/ available.

zynqmp_fsbl

TE modified 2019.2 FSBL

General:

- Modified Files: xfsbl_main.c, xfsbl_hooks.h/.c, xfsbl_board.h/.c(search for 'TE Mod' on source code)
- Add Files: te_xfsbl_hooks.h/.c (for hooks and board)\n
- General Changes:
 - Display FSBL Banner and Device Name

Module Specific:

- Add Files: all TE Files start with te_
 - Si5345 Configuration
 - OTG+PCIe Reset over MIO
 - I2C MUX for EEPROM MAC

zynqmp_fsbl_flash

TE modified 2019.2 FSBL

General:

- Modified Files: xfsbl_initialisation.c, xfsbl_hw.h, xfsbl_handoff.c, xfsbl_main.c
- General Changes:
 - Display FSBL Banner
 - Set FSBL Boot Mode to JTAG
 - Disable Memory initialisation

zynqmp_pmufw

Xilinx default PMU firmware.

hello_te0808

Hello TE0808 is a Xilinx Hello World example as endless loop instead of one console output.

u-boot

U-Boot.elf is generated with PetaLinux. Vitis is used to generate Boot.bin.

Software Design - PetaLinux

For PetaLinux installation and project creation, follow instructions from:

- [PetaLinux KICKstart](#)

Config

Start with **petalinux-config** or **petalinux-config --get-hw-description**

Select Image Packaging Configuration ==> Root filesystem type ==> Select SD Card

Changes:

- CONFIG_SUBSYSTEM_PRIMARY_SD_PSU_SD_1_SELECT=y
- CONFIG_SUBSYSTEM_ETHERNET_PSU_ETHERNET_3_MAC=""
- # CONFIG_SUBSYSTEM_BOOTARGS_AUTO is not set
- CONFIG_SUBSYSTEM_USER_CMDLINE="console=ttyPS0,115200 earlycon clk_ignore_unused earlyprintk root=/dev/mmcblk1p2 rootfstype=ext4 rw rootwait cma=1024M"
- CONFIG_SUBSYSTEM_DEVICETREE_FLAGS=""
- # CONFIG_SUBSYSTEM_IMAGES_ADVANCED_AUTOCONFIG_DTB_MEDIA_BOOTIMAGE_SELECT is not set
- # CONFIG_SUBSYSTEM_IMAGES_ADVANCED_AUTOCONFIG_DTB_MEDIA_FLASH_SELECT is not set
- CONFIG_SUBSYSTEM_IMAGES_ADVANCED_AUTOCONFIG_DTB_MEDIA_SD_SELECT=y
- # CONFIG_SUBSYSTEM_IMAGES_ADVANCED_AUTOCONFIG_DTB_MEDIA_ETHERNET_SELECT is not set
- # CONFIG_SUBSYSTEM_IMAGES_ADVANCED_AUTOCONFIG_DTB_MEDIA_MANUAL_SELECT is not set
- CONFIG_SUBSYSTEM_IMAGES_ADVANCED_AUTOCONFIG_DTB_IMAGE_NAME="system.dtb"
- CONFIG_SUBSYSTEM_ENDIAN_LITTLE=y
- # CONFIG_SUBSYSTEM_IMAGES_ADVANCED_AUTOCONFIG_KERNEL_MEDIA_FLASH_SELECT is not set
- CONFIG_SUBSYSTEM_IMAGES_ADVANCED_AUTOCONFIG_KERNEL_MEDIA_SD_SELECT=y
- # CONFIG_SUBSYSTEM_IMAGES_ADVANCED_AUTOCONFIG_KERNEL_MEDIA_ETHERNET_SELECT is not set
- # CONFIG_SUBSYSTEM_IMAGES_ADVANCED_AUTOCONFIG_KERNEL_MEDIA_MANUAL_SELECT is not set
- CONFIG_SUBSYSTEM_IMAGES_ADVANCED_AUTOCONFIG_KERNEL_IMAGE_NAME="Image"

U-Boot

Start with **petalinux-config -c u-boot**

Changes:

- CONFIG_ENV_IS_NOWHERE=y
- # CONFIG_ENV_IS_IN_SPI_FLASH is not set
- CONFIG_I2C_EEPROM=y
- CONFIG_ZYNQ_GEM_I2C_MAC_OFFSET=0xFA
- CONFIG_SYS_I2C_EEPROM_ADDR=0x50
- CONFIG_SYS_I2C_EEPROM_BUS=2
- CONFIG_SYS_EEPROM_SIZE=256
- CONFIG_SYS_EEPROM_PAGE_WRITE_BITS=0
- CONFIG_SYS_EEPROM_PAGE_WRITE_DELAY_MS=0
- CONFIG_SYS_I2C_EEPROM_ADDR_LEN=1
- CONFIG_SYS_I2C_EEPROM_ADDR_OVERFLOW=0

Device Tree

```
/include/ "system-conf.dtsi"
```

```

/ {
    chosen {
        xlnx,eeeprom = &eeeprom;
        bootargs= "console=ttyPS0,115200 earlycon clk_ignore_unused earlyprintk root=/dev/mmcblk1p2
rootfstype=ext4 rw rootwait cma=1024M";
        /* notes: root=/dev/mmcblk1p2 for SD and root=/dev/sda for hard disk will be changed
automatically by executing the debian/ubuntu script*/
    };
};

/* notes:
serdes: // PHY TYP see: dt-bindings/phy/phy.h
*/

/* default */

/* SD */

&sdhc1 {
    disable-wp;
    no-1-8-v;
};

/* USB */

&dwc3_0 {
    status = "okay";
    dr_mode = "host";
    snps,usb3_lpm_capable;
    snps,dis_u3_susphy_quirk;
    snps,dis_u2_susphy_quirk;
    phy-names = "usb2-phy","usb3-phy";
    phys = <&lane1 4 0 2 100000000>;
    maximum-speed = "super-speed";
};

/* ETH PHY */

&gem3 {
    phy-handle = <&phy0>;
    phy0: phy0@1 {
        device_type = "ethernet-phy";
        reg = <1>;
    };
};

/* QSPI */

&qspi {
    #address-cells = <1>;
    #size-cells = <0>;
    status = "okay";
    flash0: flash@0 {
        compatible = "jedec,spi-nor";
        reg = <0x0>;
        #address-cells = <1>;

```

```

        #size-cells = <1>;
    };
};

/* I2C */

&i2c0 {
    i2cswitch@73 { // u
        compatible = "nxp,pca9548";
        #address-cells = <1>;
        #size-cells = <0>;
        reg = <0x73>;
        i2c-mux-idle-disconnect;
        i2c@0 { // MCLK TEBF0808 SI5338A, 570FBB000290DG_unassembled
            #address-cells = <1>;
            #size-cells = <0>;
            reg = <0>;
        };
        i2c@1 { // SFP TEBF0808 PCF8574DWR
            #address-cells = <1>;
            #size-cells = <0>;
            reg = <1>;
        };
        i2c@2 { // PCIe
            #address-cells = <1>;
            #size-cells = <0>;
            reg = <2>;
        };
        i2c@3 { // SFP1 TEBF0808
            #address-cells = <1>;
            #size-cells = <0>;
            reg = <3>;
        };
        i2c@4 { // SFP2 TEBF0808
            #address-cells = <1>;
            #size-cells = <0>;
            reg = <4>;
        };
        i2c@5 { // TEBF0808 EEPROM
            #address-cells = <1>;
            #size-cells = <0>;
            reg = <5>;
            eeprom: eeprom@50 {
                compatible = "atmel,24c08";
                reg = <0x50>;
            };
        };
        i2c@6 { // TEBF0808 FMC
            #address-cells = <1>;
            #size-cells = <0>;
            reg = <6>;
        };
        i2c@7 { // TEBF0808 USB HUB
            #address-cells = <1>;
            #size-cells = <0>;
            reg = <7>;
        };
    };
    i2cswitch@77 { // u
        compatible = "nxp,pca9548";
        #address-cells = <1>;

```

```

#size-cells = <0>;
reg = <0x77>;
i2c-mux-idle-disconnect;
i2c@0 { // TEBF0808 PMOD P1
    #address-cells = <1>;
    #size-cells = <0>;
    reg = <0>;
};
i2c@1 { // i2c Audio Codec
    #address-cells = <1>;
    #size-cells = <0>;
    reg = <1>;

    /*
    adau1761: adau1761@38 {
        compatible = "adi,adau1761";
        reg = <0x38>;
    };
    */
};
i2c@2 { // TEBF0808 Firefly A
    #address-cells = <1>;
    #size-cells = <0>;
    reg = <2>;
};
i2c@3 { // TEBF0808 Firefly B
    #address-cells = <1>;
    #size-cells = <0>;
    reg = <3>;
};
i2c@4 { //Module PLL Si5338 or SI5345
    #address-cells = <1>;
    #size-cells = <0>;
    reg = <4>;
};
i2c@5 { //TEBF0808 CPLD
    #address-cells = <1>;
    #size-cells = <0>;
    reg = <5>;
};
i2c@6 { //TEBF0808 Firefly PCF8574DWR
    #address-cells = <1>;
    #size-cells = <0>;
    reg = <6>;
};
i2c@7 { // TEBF0808 PMOD P3
    #address-cells = <1>;
    #size-cells = <0>;
    reg = <7>;
};
};
};

```

Kernel

Start with **petalinux-config -c kernel**

Changes:

- CONFIG_CPU_IDLE is not set (only needed to fix JTAG Debug issue)
- CONFIG_CPU_FREQ is not set (only needed to fix JTAG Debug issue)
- CONFIG_EDAC_CORTEX_ARM64=y

Rootfs

Applications will be generated with Debian script or Ubuntu script (mkdebian_stretch.sh/mkubuntu_BionicBeaver.sh)

Applications

Applications will be generated with Debian script or Ubuntu script (mkdebian_stretch.sh/mkubuntu_BionicBeaver.sh)

Additional Software

No additional software is needed.

Si5345

File location <design name>/misc/Si5345/Si5345-*.slabtimeproj

General documentation how you work with these project will be available on [Si5345](#)

Appx. A: Change History and Legal Notices

Document Change History

To get content of older revision got to "Change History" of this page and select older document revision number.

Date	Document Revision	Authors	Description
<div><div>Error rendering macro 'page-info'</div><div>Ambiguous method overloading for method jdk.proxy241.\$Proxy3496#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface</div></div>	<div><div>Error rendering macro 'page-info'</div><div>Ambiguous method overloading for method jdk.proxy241.\$Proxy3496#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface</div></div>	<div><div>Error rendering macro 'page-info'</div><div>Ambiguous method overloading for method jdk.proxy241.\$Proxy3496#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface</div></div>	<div><div>• Typo</div></div>

<p>com.atlassian.confluence.user. ConfluenceUser, class java. lang.String, class com. atlassian.confluence.core. ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core. ContentEntityObject]</p>	<p>com.atlassian.confluence.user. ConfluenceUser, class java. lang.String, class com. atlassian.confluence.core. ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core. ContentEntityObject]</p>	<p>com.atlassian.confluence.user. ConfluenceUser, class java. lang.String, class com. atlassian.confluence.core. ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com. atlassian.confluence.core. ContentEntityObject]</p>	
2020-05-11	v.1	Mohsen Chamanbaz	<ul style="list-style-type: none"> 2019.2 release
--	all	<p>Error rendering macro 'page-info'</p> <p>Ambiguous method overloading for method jdk.proxy241.\$Proxy3496#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]</p>	--

Document change history.

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Please also note our data protection declaration at <https://www.trenz-electronic.de/en/Data-protection-Privacy>

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