TE0724 TRM

Table of Contents

Overview

The Trenz Electronic TE0724 is an industrial-grade SoC module based on Xilinx Zynq 7010/7020, which provides a dual core ARM Cortex A9 and a 7-series FPGA logic. It provides a gigabit ethernet transceiver, 1 GByte of DDR3L SDRAM, 64 MByte Flash memory as configration and data storage. It includes strong power regulators for all needed voltages and a robust high-speed connector for in- and outputs. It has a 6 x 4 cm form factor.

Key Features

- Xilinx Zynq XC7Z010-1CLG400I or XC7Z020-1CLG400I
  - Dual-core ARM Cortex-A9 MPCore
  - Max. 667 MHz
- Shock proof and vibration resistant
- Size 6 x 4 cm
- Plug-On-Modul with 1 × 160 Pin High-Speed connector
- 1 GByte DDR3L SDRAM
- 64 MByte QSPI Flash Speicher
- 1 x GBit Ethernet PHY
- 1 x MAC-Address EEPROM
- 128 KBit EEPROM
- 1 x CAN Transceiver
- On-Board DC/DC-regulators
- Excellent signal integrity due to evenly-spread supply pins

Additional assembly options are available for cost or performance optimization upon request.

Block Diagramm

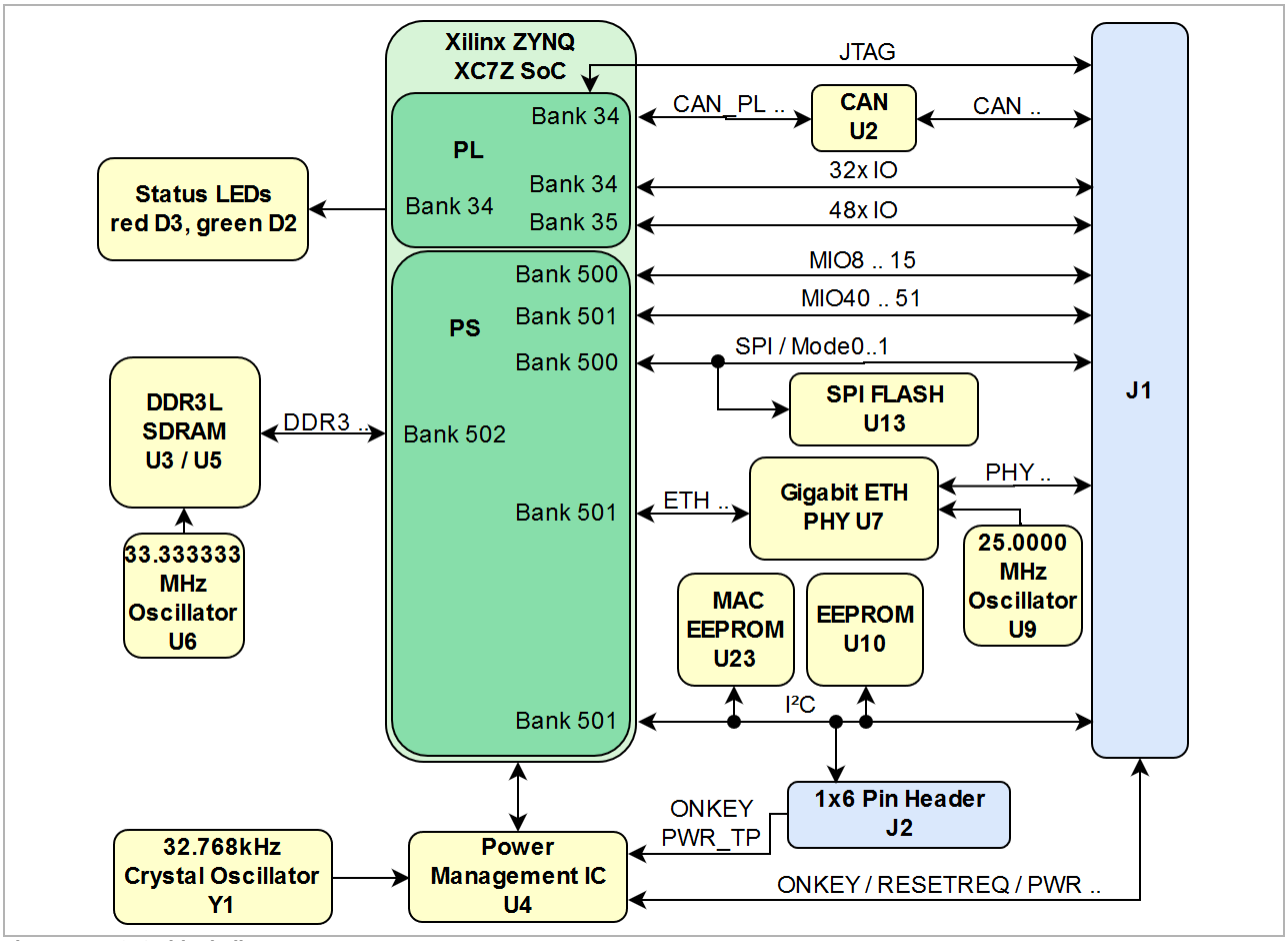
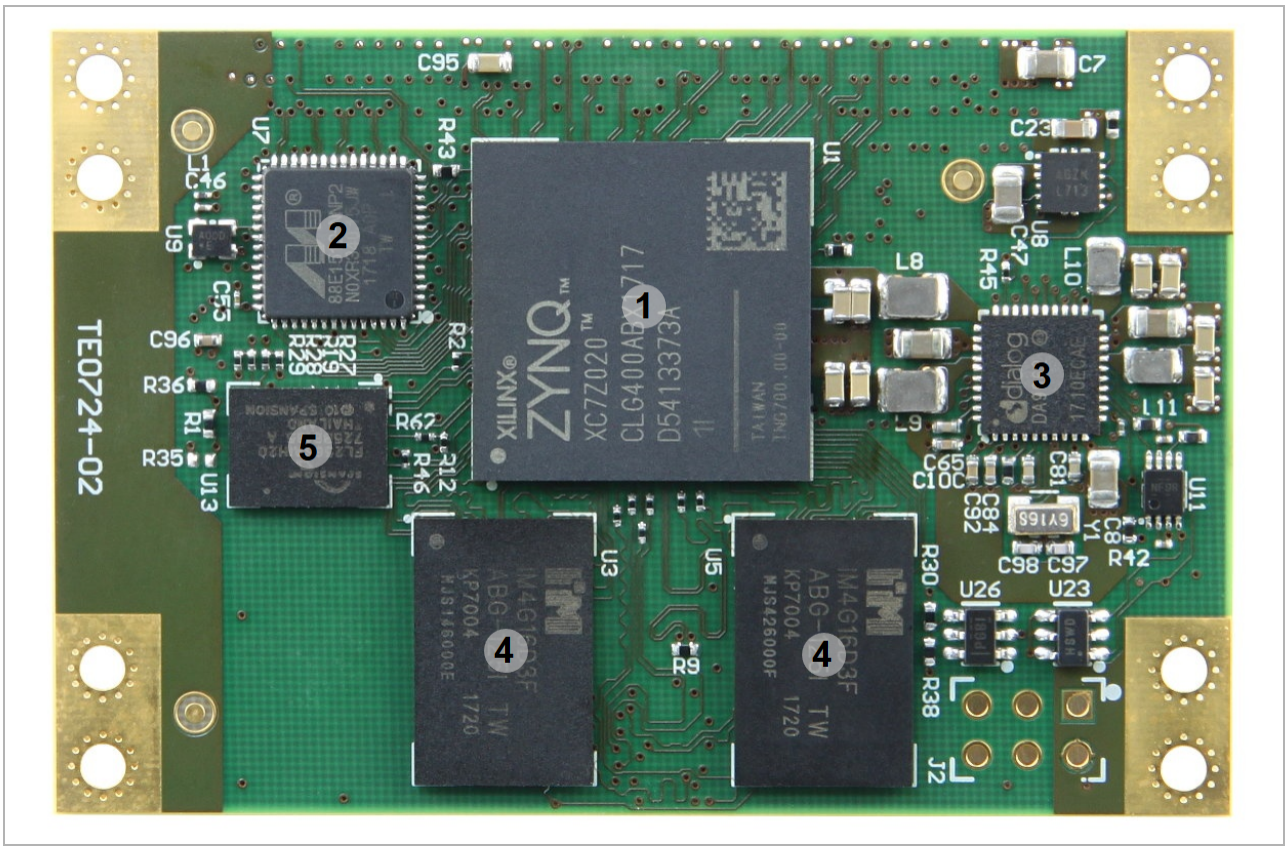


Figure 1: TE0724 block diagram

Main Components


TE0724-02
1
2
3
4
4
5
XILINX
ZYNQ
XC7Z020
CLG400AB
D5413373A
TAIWAN
C95
C7
C23
U7
R43
U1
C46
U9
C55
C96
R36
R1
R35
U13
R62
R46
R12
C65
C10
C81
C84
C92
C98
C97
C8
Y1
R42
U11
L8
L10
L11
R45
U8
C47
U26
U23
R30
R38
J2
U3
U5
R9

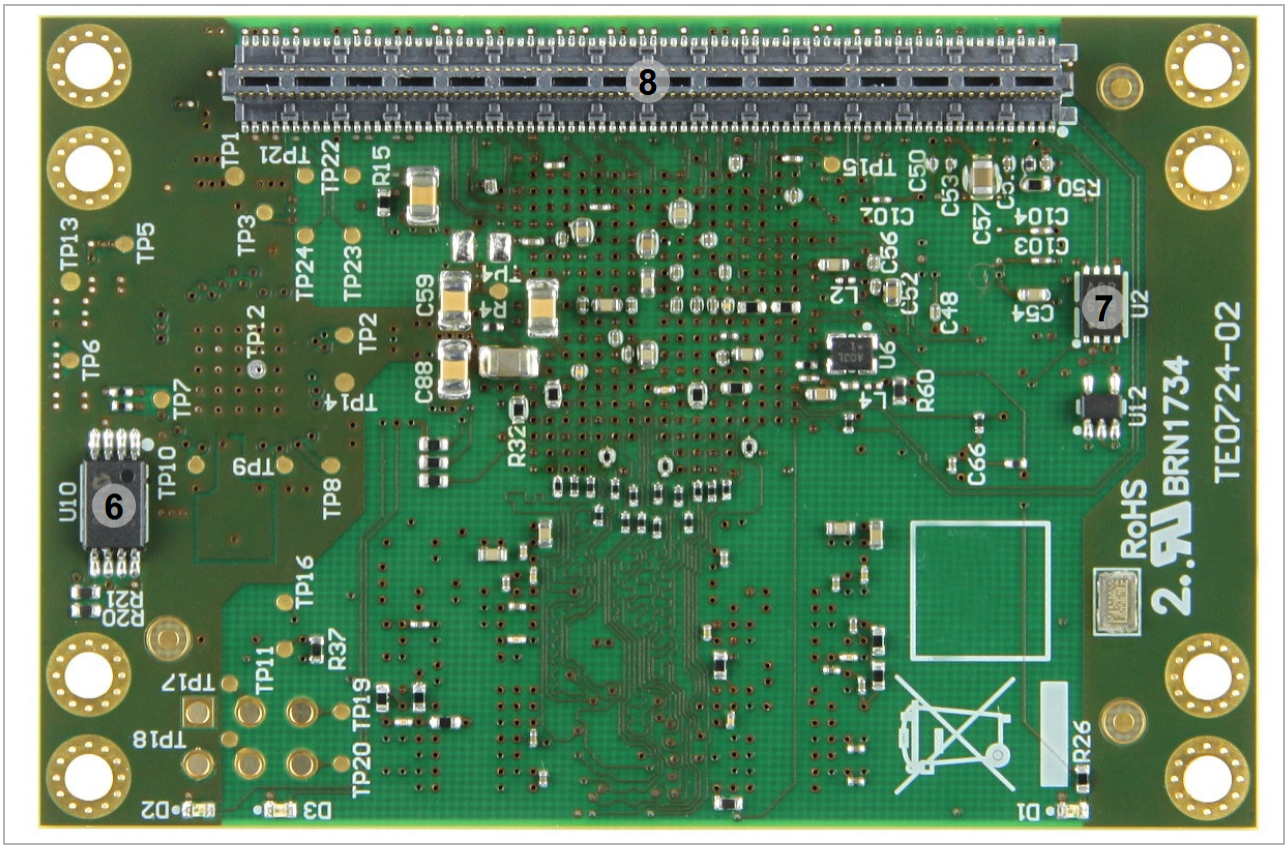


Figure 2: TE0724 main components

1. XILINX ZYNQ XC7Z020-2CLG400C, U1
2. Gigabit Ethernet Transceiver Alaska 88E1512, U7
3. Power Manager Dialog DA9062, U4
4. 1GByte - 2x 4Gbit DDR3L RAM, U3, U5
5. 64MByte ISSI SPI Flash IS25LP512M, U13
6. 128KByte Serial EEPROM Microchip 24AA, U10
7. CAN Transceiver MCP2542FDT, U2
8. 160 Pin Samtec B2B Connector ST5-80-1.50-L-D-P-TR, J1

Initial Delivery State

Storage device name	Content	Notes
ISSI SPI Flash IS25LP512M, U13	Empty	
DA9062, U4	Programmed	
Microchip 24AA128T, U10	Empty	USER EEPROM
Microchip 24AA025E48T, U23	MAC write protected preprogrammed, User area empty	EEPROM for MAC-Address.

Table 1: Initial delivery state of programmable devices on the module.

Boot Process

Boot mode is selected via two Mode pins at B2B connector J2. By default the TE0724 supports JTAG and SPI Boot Mode. Connecting a SD Card via B2B connector to MIO Pins (See SD Card Interface) gives the possibility to boot from SD Card. The Mode pins are pulled up at the module.

Boot mode	MODE1 J1-2	MODE0 J1-4
JTAG (cascade)	LOW	LOW
invalid	LOW	HIGH
SPI	HIGH	LOW
SD CARD (not on module)	HIGH	HIGH

Table 2: Boot mode selection.

Signals, Interfaces and Pins

Board to Board (B2B) I/Os

I/O signals connected to the SoCs I/O bank and B2B connector:

Bank	Type	B2B Connector	I/O Signal Count	Bank Voltage	Notes
500	MIO	J1	8 I/Os	3.3V	On-module power supply.
501	MIO	J1	12 I/Os	1.8V	On-module power supply.
34	HR	J1	32 I/Os or 16 LVDS pairs	3.3V	On-module power supply.
35	HR	J1	48 I/Os or 24 LVDS pairs	VCCIO_35	Supplied by the carrier board.

Table 3: General overview of PL I/O signals connected to the B2B connectors.

All PS MIO banks as well as PL bank 34 are powered by on-module DC-DC power rails. Valid VCCO_35 for PL bank 35 should be supplied via the B2B connector.

For detailed information about the pin out, please refer to the Pin-out Tables.

The configuration of the PS I/Os MIO40 to MIO51 depend on the carrier board peripherals connected to these pins.

JTAG Interface

JTAG access to the ZYNQ SoC is provided through B2B connector J1 and testpoints.

JTAG Signal	B2B Connector Pin
TCK	J1-147
TDI	J1-151
TDO	J1-145
TMS	J1-149

Table 4: JTAG interface signals.

System Controller Pins

Special purpose pins are available for System Controller functions and are routed to the Power Management IC (U4) with the following default configuration:

Signal Name	Mode	Function	B2B Connector Pin	Configuration
RESETREQ	INPUT	Reset request	J1-150	Aktive LOW, enter reset mode when set low. Pulled up to VIN.
ONKEY	INPUT	Power-on key	J1-148	Debounced edge sensitve power mode manipulator. On/Off with optional long press shutdown, function dependent on register value of NONKEY_PIN, KEY_DELAY.
PWR_TP	IN/OUT	Test pin	J1-146	Enables Power Commander boot mode and supply pin for OTP fusing voltage.
PWR_GPIO2	IN/OUT		J1-143	
PWR_GPIO2	IN/OUT		J1-141	

Table 5: System Controller CPLD I/O pins.

Quad SPI Interface

Quad SPI Flash (U13) is connected to the Zynq PS QSPI_0 interface via PS MIO bank 500, pins MIO1 ... MIO6.

MIO	Signal Name	U14 Pin
1	SPI_CS	C2
2	SPI_DQ0/MIO2	D3
3	SPI_DQ1/MIO3	D2
4	SPI_DQ2/MIO4	C4
5	SPI_DQ3/MIO5	D4
6	SPI_SCK/MIO6	B2

Table 6: Quad SPI interface signals and connections.

SD Card Interface

There is no physical SD Card slot on the module. Three different interface options are possible at a carrier via the PS MIO 10 to 15 or 40 to 45 or 46 to 51 plus additional MIOs for SD Card Detect and Write Protect as well as SD Card Power Controls. For details compare Xilinx UG585-Zynq-7000-TRM Table 2-4.

Ethernet Interface PHY

The TE0724 is equipped with a Marvell Alaska 88E1512 Gigabit Ethernet PHY (U7) connected to PS Ethernet GEM0. The I/O Voltage is fixed at 1.8V for HSTL signaling. The reference clock input of the PHY is supplied from an on-board 25.000000 MHz oscillator (U9), the 125MHz output clock signal CLK_125MHZ is connected to the PL IO_L11P_T1_SRCC_34.

PHY Pin	PS bank 501	B2B	Notes
MDC/MDIO	MIO52/MIO53	-	
LED0	-	J1-10	

LED1	-	J1-12	
LED2/Interrupt	-	-	not connected
CONFIG	-	-	connected to 1.8V (VDDO), PHY Address = 1
RESETn	MIO39	-	
RGMII	MIO16..MIO27	-	
SGMII	-	-	not connected
MDI	-	J1-7,9,13,15,19,21,25,27	

Table 7: Ethernet PHY connections.

CAN PHY

A felxible data rate CAN Transceiver is provided by a Microchip MCP2542FDT.

PHY Pin	PL bank 34	B2B	Notes
TX/RX	IO_L1P/IO_L1N	-	
CAN_L / CAN_H	-	J1-1 / J1-3	

Table 8: CAN PHY connections.

I2C Interface

On-board I^2C devices are connected to PS MIO28 (SCL) and MIO29 (SDA). I^2C addresses for on-board devices are listed in the table below:

I2C Device	7bit I2C Address	Notes
MAC EEPROM, U23	0x53	1.8V
USER EEPROM, U10	0x50	1.8V
Power Management U4	0x58 / 0x59	3.3V
J1	-	J1-142 SDA, J1-144 SDL at 3.3V

Table 9: I^2C slave device addresses.

On-board Peripherals

Power Management IC

The power management IC (U4) is provided by dialog Semiconductors (DA9062). It controls the power-on sequencing of the various power rails. It is preprogrammed and accessible via I^2C address 0x58 / 0x59. For a detailed description of the configurable power management IC please refer to the datasheet of dialog semicondutor DA9062.

DDR Memory

By default TE0724 module has 2 DDR3L SDRAM chips arranged into 32-bit wide memory bus providing total of 1 GBytes of on-board RAM. Different memory sizes are available optionally.

Quad SPI Flash Memory

On-board QSPI flash memory (U13) on the TE0724-04 is a ISSI IS25LP512M with 512 Mbit (64 MByte) storage capacity. This non volatile memory is used to store initial FPGA configuration. Besides FPGA configuration, remaining free flash memory can be used for user application and data storage. All four SPI data lines are connected to the FPGA allowing x1, x2 or x4 data bus widths. Maximum data rate depends on the selected bus width and clock frequency used.

> ⚠ SPI Flash QE (Quad Enable) bit must be set to high or FPGA is unable to load its configuration from flash during power-on. By default this bit is set to high at the manufacturing plant.

MAC Address EEPROM

A Microchip 24AA025E48 serial EEPROM (U23) contains a globally unique 48-bit node address, which is compatible with EUI-48(TM) specification. The device is organized as two blocks of 128 x 8-bit memory. One of the blocks stores the 48-bit node address and is write protected, the other block is available for application use. It is accessible over I^2C bus with slave device address 0x53.

> ⚠ Max. I2C Speed for 24AA025E48 EEPROM is 100kHz.

USER EEPROM

A Microchip 24AA128T serial EEPROM (U10) is available for e.g. module identification and user Data. The device has 128Kbit memory with max 64 bytes page write capability. It is accessible over I^2C bus with slave device address 0x50.

> ⚠ Max. I2C Speed for 24AA128T EEPROM is 100kHz.

Oscillators

The module has following reference clock signals provided by on-board oscillators and external source from carrier board:

Clock Source	Schematic Signal	Frequency	Clock Destination
SiTime SiT8008BI oscillator, U9	ETH_XTAL	25.000000 MHz	XTAL_IN, U7 ETH PHY
SiTime SiT8008AI oscillator, U6	PS_CLK	33.333333 MHz	PS_CLK_500, Bank 500

Table10 : Reference clock signals.

On-board LEDs

LED	Color	Connected to	Description and Notes
D1	Green	PS MIO7	User LED.
D2	Green	PL IO_L3P_T0_34	User LED.
D3	Red	PL IO_L4N_T0_34	User LED.

Table 11: On-board LEDs.

Pin Header

Optional assembled Pin Header J2 can be used for PMIC In-System Programming.

Pin	Signal	B2B
J2-1	VIN	J1-154, J1-156, J1-158, J1-160
J2-2	GND	
J2-3	I2C_SCL	J1-142
J2-4	I2C_SDA	J1-144
J2-5	ONKEY	J1-148
J2-6	PWR_TP	J1-146

Table 12: Optional assembled Pin Header.

Power and Power-On Sequence

Power Consumption

The maximum power consumption of a module mainly depends on the design running on the FPGA.

Xilinx provide a power estimator excel sheets to calculate power consumption. It's also possible to evaluate the power consumption of the developed design with Vivado. See also Trenz Electronic Wiki FAQ.

Power Input	Typical Current
VIN	TBD*

Table 13: Typical power consumption.

* TBD - To Be Determined soon with reference design setup.

Power supply with minimum current capability of ...A for system startup is recommended.

The on-board voltages of the TE0724 SoC module will be powered-up in order of a determined sequence after the external voltages VIN is available and nONKEY is asserted.

To avoid any damage to the module, check for stabilized on-board voltages should be carried out (i.e. power good and enable signals) before powering up any SoC's I/O bank voltages VCCO_x. All I/Os should be tri-stated during power-on sequence.

Power Distribution Dependencies

DCDC U8 component is either TPS82140 (2 A) or MUN12A (3 A) depending on the variant.

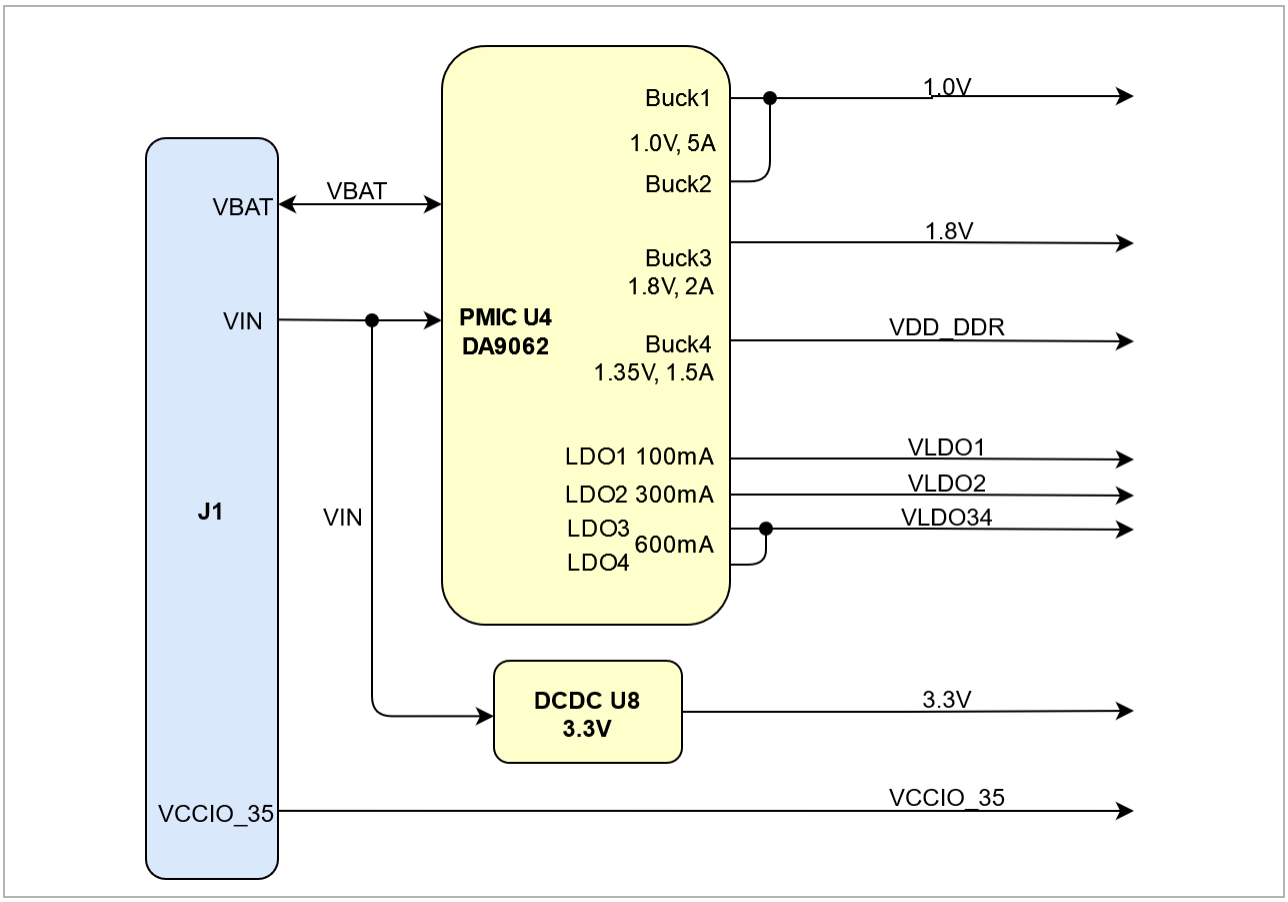


Figure 3: TE0724 power distribution diagram.

See Xilinx data sheet for additional information. User should also check related base board documentation when intending base board design for TE0724 module.

Power-On Sequence

The TE0724 SoM meets the recommended criteria to power up the Xilinx Zynq MPSoC properly by keeping a specific sequence of enabling the on-board DC-DC converters dedicated to the particular functional units of the Zynq chip and powering up the on-board voltages. For a detailed description of the configurable Power Management IC please refer to the datasheet of dialog semicondutor DA9062.

Following diagram clarifies the sequence of enabling the particular on-board voltages, which will power-up in ascending order as listed in the blocks of the diagram:

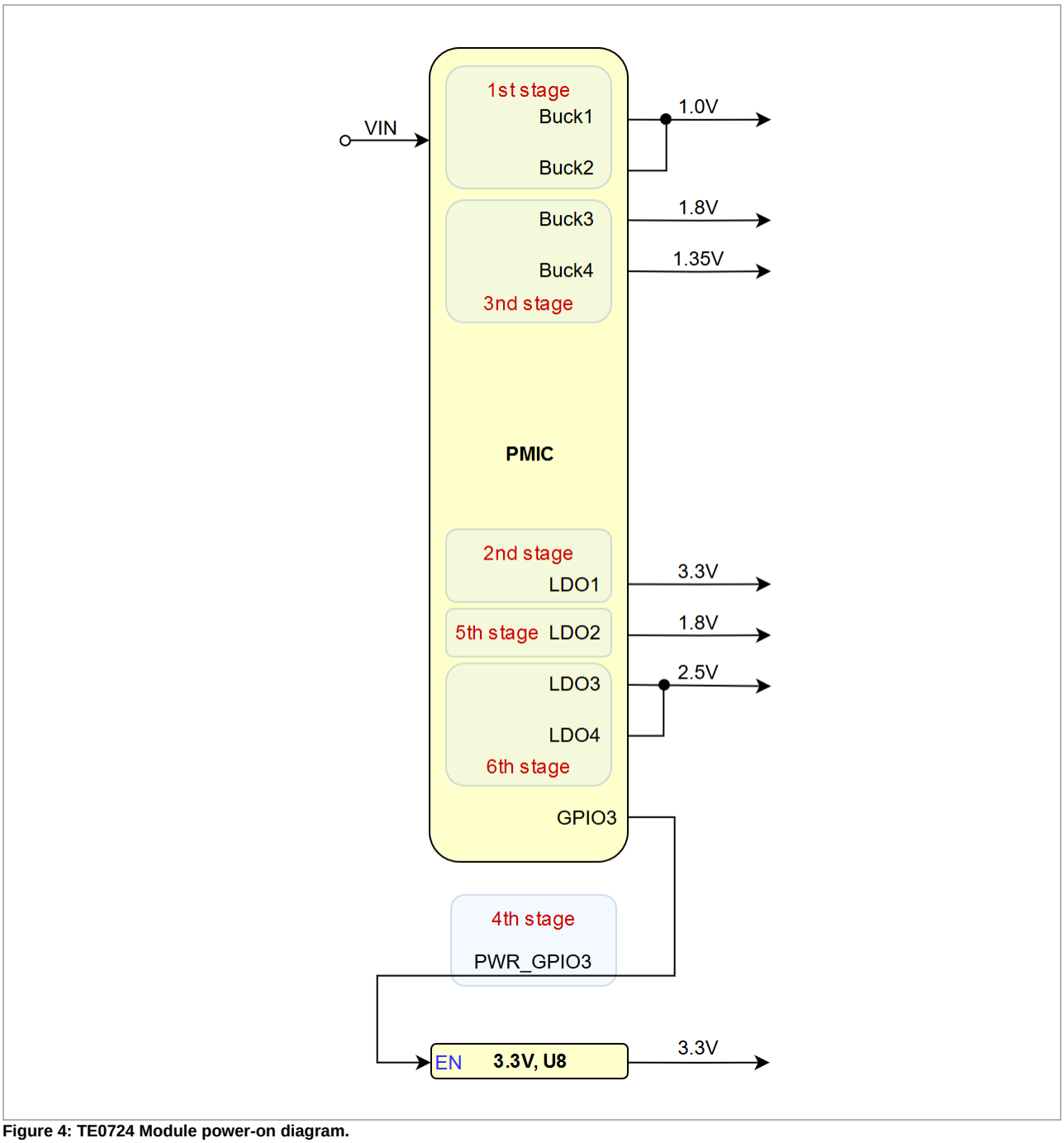


Figure 4: TE0724 Module power-on diagram.

Power Rails

Power Rail Name	B2B JM1 Pins	Direction	Notes
VIN	154, 156, 158,160	Input	Main supply voltage from the carrier board.

VCCIO_35	54	Input	PL Bank 35 supply voltage.
VLDO1	83	Output	3.3V (100mA)
VLDO2	94	Output	1.8V (300mA)
VLDO34	53	Output	2.5V (600mA)
3.3V	43, 74	Output	Additional module on-board 3.3V voltage supply (2 A or 3 A variant dependent).
1.0V	-		Buck1 & Buck2 of U4.
1.8V	63	Output	Buck3 of U4.
VDD_DDR	-		DDR supply voltage powered by Buck4 of U4.
VBAT	152	Output/Input	Battery charger (out) and supply for RTC and 32kHz crystal (in).

Table 14: Module power rails.

Current rating of the Samtec connector is 1.6A per pin (1 pin powered per row).

Bank Voltages

Bank	Schematic Name	Voltage	Voltage Range
500 MIO	3.3V	3.3V	-
501 MIO	1.8V	1.8V	-
502 DDR3	VDD_DDRV	1.35V	-
34 HR	3.3V	3.3V	-
35 HR	VCCIO_35	User	1.2V to 3.3V

Table 15: Module PL I/O bank voltages.

Board to Board Connectors

The module has a 160-pin double-row REF-192552-02 connector on the bottom side. The counterpart REF-192552-01 is placed on the base board.

Order number	REF Number	Samtec Number	Type	Mated Height	Data sheet	Comment
27220	REF-192552-02	ST5-80-1.50-L-D-P-TR	Module connector	5 mm	http://suddendocs.samtec.com/catalog_english/st5.pdf	Standard connector used on module
27219	REF-192552-01	SS5-80-3.50-L-D-K-TR	Baseboard connector	5 mm	http://suddendocs.samtec.com/catalog_english/ss5.pdf	Standard connector used on board

Connectors.

With different connectors from the used series other mating heights are possible (according to the Datasheet). The module and base board can be manufactured using other connectors upon request.

Connector Specifications	Value
Insulator material	Liquid crystal polymer
Stacking height	5 mm
Contact material	Phosphor-bronze

Plating	Au or Sn over 50 " (1.27 m) Ni
Current rating	1.6 A per pin (2 pins powered)
Operating temperature range	-55 °C to +125 °C
RoHS compliant	Yes

Connector specifications.

Connector Speed Ratings

The LSHM connector speed rating depends on the stacking height; please see the following table:

Stacking height	Speed rating
5 mm, Single-Ended	13.5GHz / 27Gbps
5 mm, Differential	20GHz / 40Gbps
4 mm, Single-Ended	13GHz / 26Gbps
4 mm, Differential	13.5GHz / 27Gbps

Speed rating.

Current Rating

Current rating of Samtec Razor Beam™ SS5/ST5 B2B connectors is 1.6A per pin (2 pins powered).

Connector Mechanical Ratings

- Shock: 100G, 6 ms sawtooth wave
- Vibration: 7.56G 'RMS', 2 hours per axis, 3 axes total

Manufacturer Documentation

File	Modified
PDF File hsc-report-sma_st5-ss5-04mm_web.pdf	21 09, 2018 by Martin Rohrmüller
PDF File hsc-report-sma_st5-ss5-05mm_web.pdf	21 09, 2018 by Martin Rohrmüller
PDF File ss5_catalog.pdf	21 09, 2018 by Martin Rohrmüller
PDF File ss5-st5_specs.pdf	21 09, 2018 by Martin Rohrmüller

Download All

Variants Currently In Production

Trenz shop TE0724 overview page	
English page	German page

Technical Specifications

Absolute Maximum Ratings

Parameter	Min	Max	Units	Reference Document
VIN supply voltage	-0.3	5.5	V	da9062_3v4.pdf
Storage temperature	-40	85	°C	-

Table 18: Module absolute maximum ratings.

⚠ Assembly variants for higher storage temperature range are available on request.

Recommended Operating Conditions

Parameter	Min	Max	Units	Reference Document
VIN supply voltage (variant "-Z" with MUN12A for U8)	4.5	5.5	V	
VIN supply voltage (all other variants)	3.6	5.5	V	
Operating temperature	-40	85	°C	

Table 19: Module recommended operating conditions.

⚠ Please check Xilinx datasheet ... for complete list of absolute maximum and recommended operating ratings.

Operating Temperature Ranges

Commercial grade: 0°C to +70°C.

Extended grade: 0°C to +85°C.

Industrial grade: -40°C to +85°C.

Module operating temperature range depends also on customer design and cooling solution. Please contact us for options.

Physical Dimensions

- Module size: 60 mm × 40 mm. Please download the assembly diagram for exact numbers.
- Mating height with standard connectors: 5.0 mm.
- PCB thickness: 1.6 mm.
- Highest part on PCB: approx. 1.6 mm. Please download the step model for exact numbers.

All dimensions are given in millimeters.

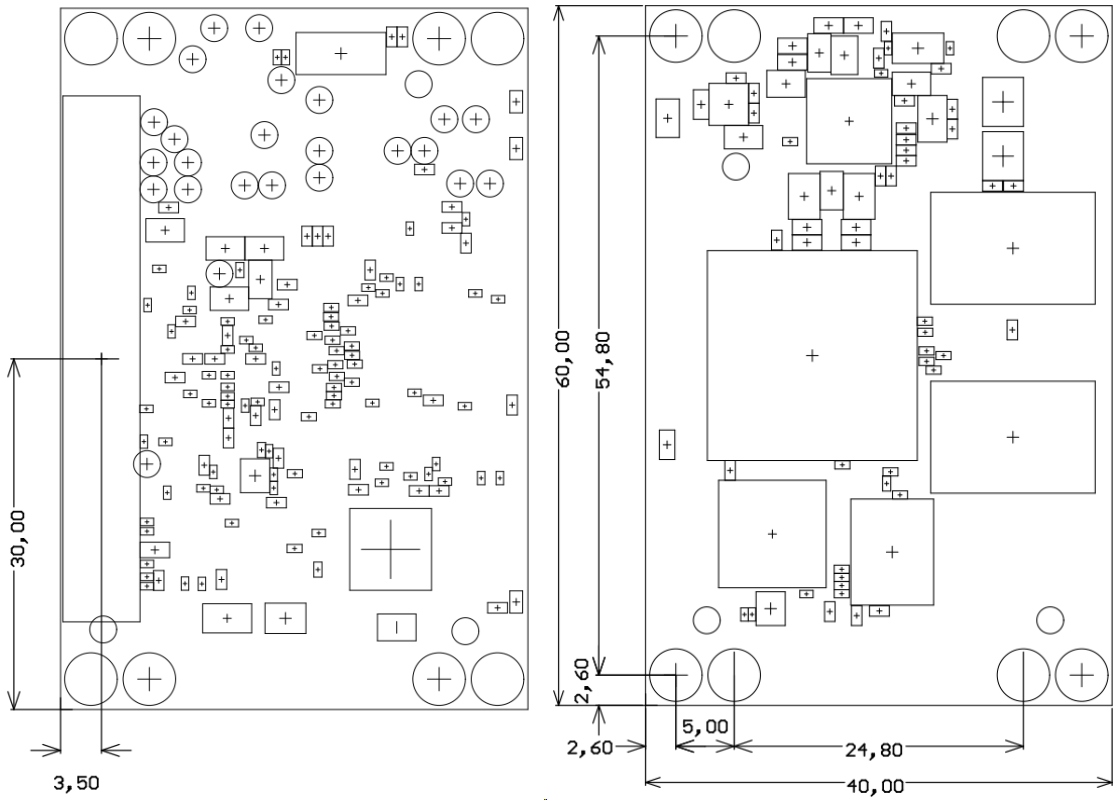


Figure 5: TE0724 Mechanical Dimensions.

Revision History

Hardware Revision History

Date	Revision	Notes
2020-11-05	04	Changed DDR3, Flash, see PCN
2019-03-12	03	changed 3.3V DCDC
	02A	Electrical same as REV 02.
	02	First production release
-	01	Prototypes

Table 20: Module hardware revision history.

Hardware revision number can be found on the PCB board together with the module model number separated by the dash.

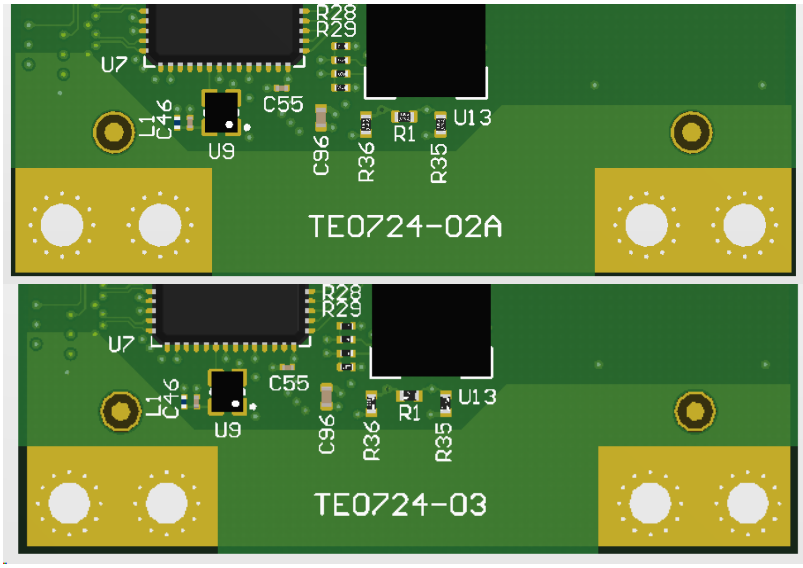


Figure 6: TE0724 module hardware revision number.

Document Change History

Date	Revision	Contributors	Description

Error rendering macro 'page-info' Ambiguous method overloading for method jdk.proxy241.$Proxy3496#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]	**Error rendering macro 'page-info'** Ambiguous method overloading for method jdk.proxy241.$Proxy3496#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]	**Error rendering macro 'page-info'** Ambiguous method overloading for method jdk.proxy241.$Proxy3496#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]	• update for "-Z" variant (MUN12A)
2020-11-17	v.58	Martin Rohrmüller	• update to REV04 (DDR, Flash)
2019-10-31	v.56	Martin Rohrmüller	• VBAT is In/OUT (charger)
2019-10-30	v.55	John Hartfield	• correction on power section

2019-06-27	v.54	Martin Rohrmüller	• Updated Power Distribution dependencies Figure (VBAT: Charge and Use)
2019-06-11	v.53	Guillermo Herrera	• typo correction on Bank voltage section
2019-03-29	v.51	Martin Rohrmüller	• update to REV03
2018-11-20	v.44	John Hartfiel	• remove typo
2018-10-10	v.43	John Hartfiel	• Add notes to EEPROM section
2018-10-09	v.42	Martin Rohrmüller	• corrected mating high at physical dimensions
2018-10-01	v.41	Martin Rohrmüller	• corrected typo in power up order • updated B2B power rating
2018-09-21	v.39	Martin Rohrmüller	• B2B Connectors as include from general page
2018-07-20	v.37	John Hartfield	• small style changes

2018-07-06	v.34	Martin Rohrmüller	• Initial document.
---	all	**Error rendering macro 'page-info'** Ambiguous method overloading for method jdk.proxy241.$Proxy3496#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]	• ---

Table 21: Document change history.

Disclaimer

Data Privacy

Please also note our data protection declaration at https://www.trenz-electronic.de/en/Data-protection-Privacy

Document Warranty

The material contained in this document is provided “as is” and is subject to being changed at any time without notice. Trenz Electronic does not warrant the accuracy and completeness of the materials in this document. Further, to the maximum extent permitted by applicable law, Trenz Electronic disclaims all warranties, either express or implied, with regard to this document and any information contained herein, including but not limited to the implied warranties of merchantability, fitness for a particular purpose or non infringement of intellectual property. Trenz Electronic shall not be liable for errors or for incidental or consequential damages in connection with the furnishing, use, or performance of this document or of any information contained herein.

Limitation of Liability

In no event will Trenz Electronic, its suppliers, or other third parties mentioned in this document be liable for any damages whatsoever (including, without limitation, those resulting from lost profits, lost data or business interruption) arising out of the use, inability to use, or the results of use of this document, any documents linked to this document, or the materials or information contained at any or all such documents. If your use of the materials or information from this document results in the need for servicing, repair or correction of equipment or data, you assume all costs thereof.

Copyright Notice

Technology Licenses

The hardware / firmware / software described in this document are furnished under a license and may be used /modified / copied only in accordance with the terms of such license.

Environmental Protection

To confront directly with the responsibility toward the environment, the global community and eventually also oneself. Such a resolution should be integral part not only of everybody's life. Also enterprises shall be conscious of their social responsibility and contribute to the preservation of our common living space. That is why Trenz Electronic invests in the protection of our Environment.

REACH, RoHS and WEEE

REACH

Trenz Electronic is a manufacturer and a distributor of electronic products. It is therefore a so called downstream user in the sense of REACH. The products we supply to you are solely non-chemical products (goods). Moreover and under normal and reasonably foreseeable circumstances of application, the goods supplied to you shall not release any substance. For that, Trenz Electronic is obliged to neither register nor to provide safety data sheet. According to present knowledge and to best of our knowledge, no SVHC (Substances of Very High Concern) on the Candidate List are contained in our products. Furthermore, we will immediately and unsolicited inform our customers in compliance with REACH - Article 33 if any substance present in our goods (above a concentration of 0,1 % weight by weight) will be classified as SVHC by the European Chemicals Agency (ECHA).

RoHS

Trenz Electronic GmbH herewith declares that all its products are developed, manufactured and distributed RoHS compliant.

WEEE

Information for users within the European Union in accordance with Directive 2002/96/EC of the European Parliament and of the Council of 27 January 2003 on waste electrical and electronic equipment (WEEE).

Users of electrical and electronic equipment in private households are required not to dispose of waste electrical and electronic equipment as unsorted municipal waste and to collect such waste electrical and electronic equipment separately. By the 13 August 2005, Member States shall have ensured that systems are set up allowing final holders and distributors to return waste electrical and electronic equipment at least free of charge. Member States shall ensure the availability and accessibility of the necessary collection facilities. Separate collection is the precondition to ensure specific treatment and recycling of waste electrical and electronic equipment and is necessary to achieve the chosen level of protection of human health and the environment in the European Union. Consumers have to actively contribute to the success of such collection and the return of waste electrical and electronic equipment. Presence of hazardous substances in electrical and electronic equipment results in potential effects on the environment and human health. The symbol consisting of the crossed-out wheeled bin indicates separate collection for waste electrical and electronic equipment.

Trenz Electronic is registered under WEEE-Reg.-Nr. DE97922676.

Error rendering macro 'page-info'

Ambiguous method overloading for method jdk.proxy241.$Proxy3496#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]