TEB0835 TRM

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Overview

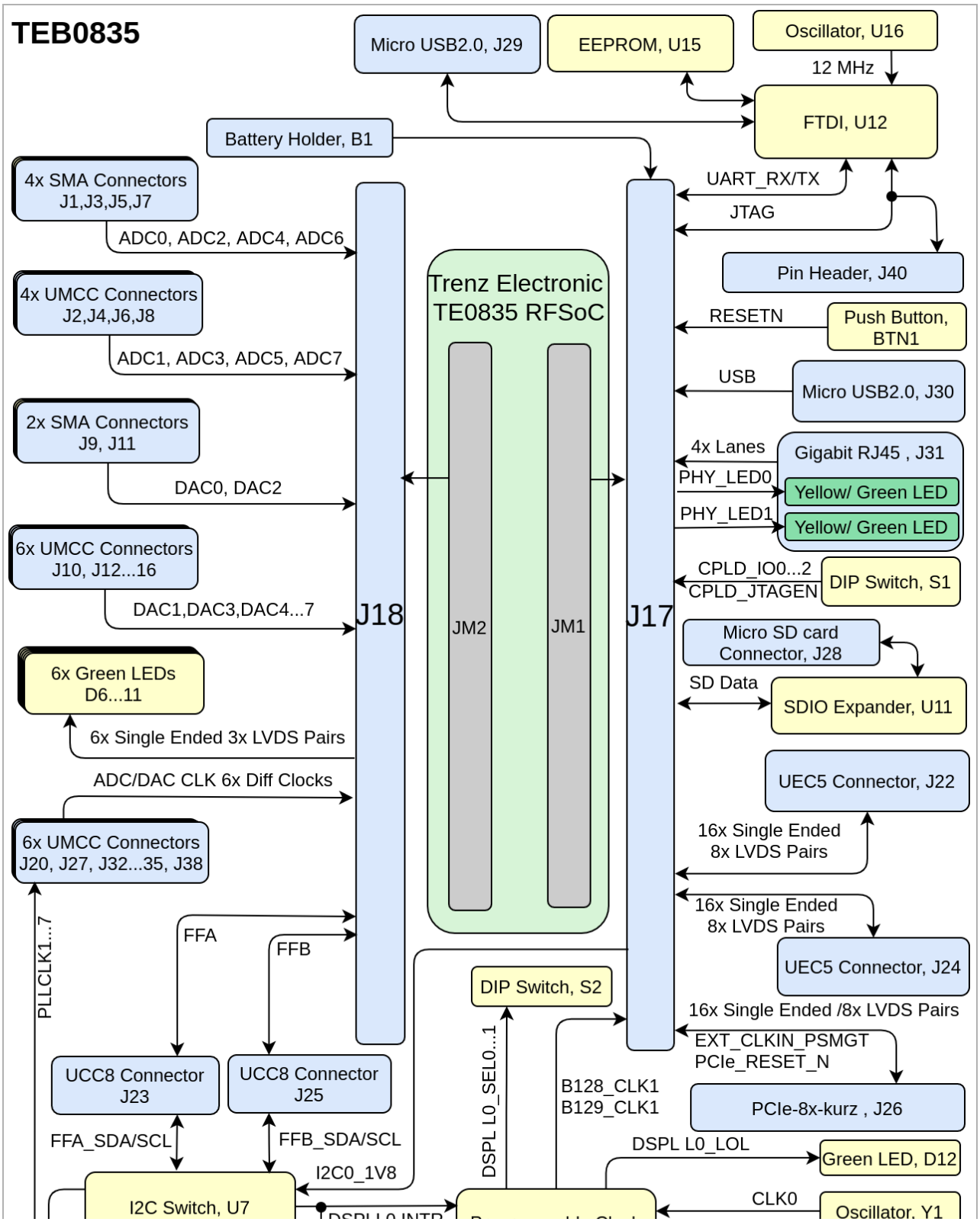
The Trenz Electronic TEB0835 is a carrier for TE0835 module which is based on Xilinx UltraScale+ RFSoC. The Carrier is equipped with a Micro SD card reader, Micro USB2.0, 21x UMCC connectors and 6x SMA connectors for clocks and ADC/DAC inputs/outputs , 6x Green User LEDs, Reset Push Button, DIP Switch for Mode, Battery Holder, FT2232H FTDI, programmable clock generators and a Temperature sensor IC. The carrier provides PCIe connector as well.

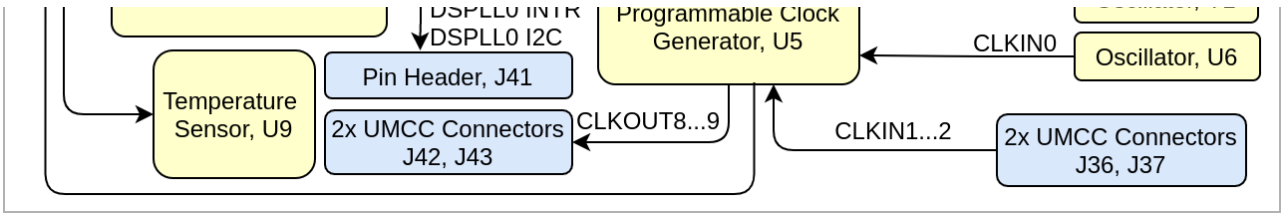
Refer to http://trenz.org/teb0835-info for the current online version of this manual and other available documentation.

Key Features

- **Modules:**
  - TE0835
- **RAM/Storage**
  - 4 GB DDR4 RAM
- **On Board**
  - Programmable Clock Generator
  - I²C Switch IC
  - 6x User Green LEDs
  - 16x RF Transformation
  - Reset Push Button
  - Temperature Sensor
  - FT2232H FTDI
  - SDIO Port Expander
  - 2x DIP Switch
  - Pin Headers
  - PCIe 8 Connector
- **Interface**
  - 21x UMCC Connectors
  - 6x SMA Connectors
  - 2X Micro USB2.0
  - RJ45 LAN Socket
  - Micro SD Card Socket
  - 2x UCC5 Connectors
  - 2x UCC8 Connectors
  - PCIe x8 Card
  - 2x Samtec Razor Beam SS5 (2x80 pol) Board to Board Connectors
- **Power**
  - 12V Input Supply Voltage
- **Dimension**
  - 106.6 x 167.6 mm

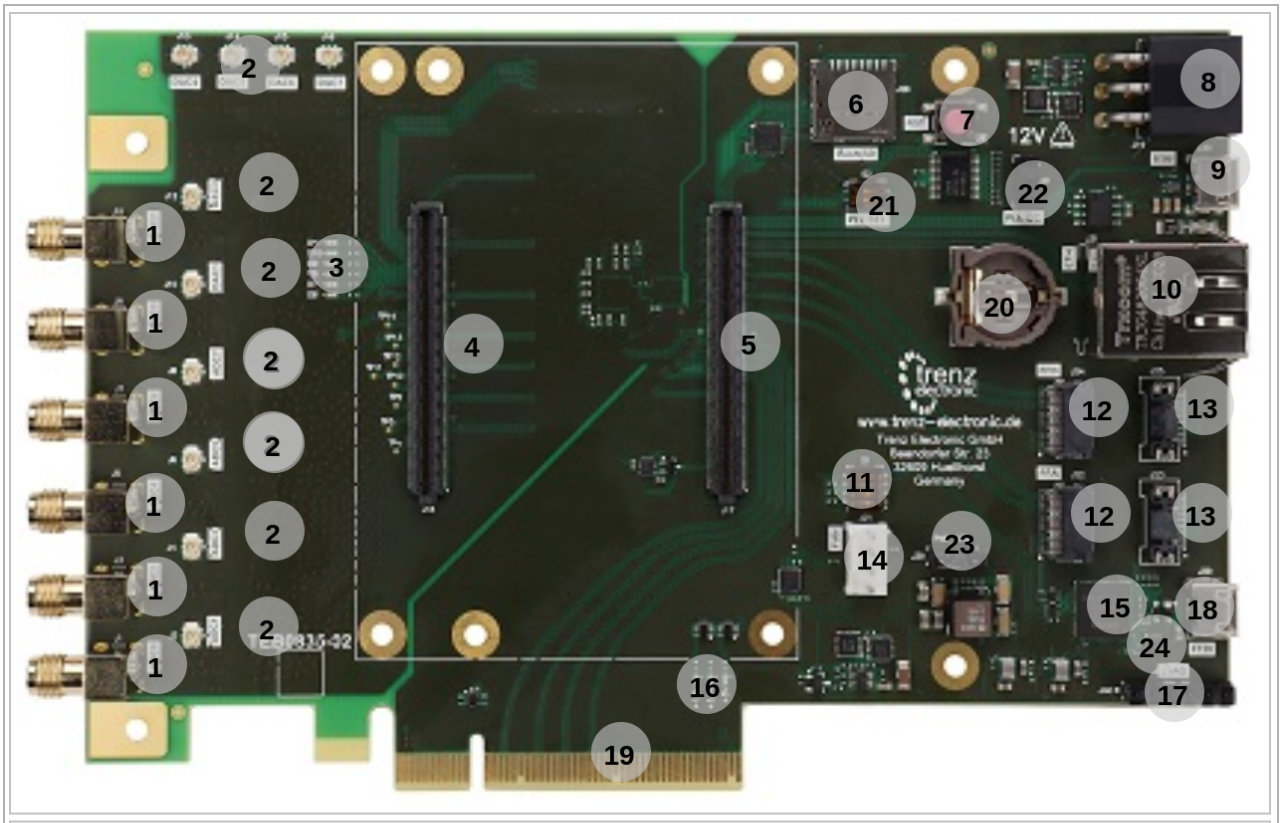
Block Diagram


TEB0835
Micro USB2.0, J29
EEPROM, U15
Oscillator, U16
12 MHz
FTDI, U12
Battery Holder, B1
4x SMA Connectors J1,J3,J5,J7
ADC0, ADC2, ADC4, ADC6
4x UMCC Connectors J2,J4,J6,J8
ADC1, ADC3, ADC5, ADC7
2x SMA Connectors J9, J11
DAC0, DAC2
6x UMCC Connectors J10, J12...16
DAC1,DAC3,DAC4...7
6x Green LEDs D6...11
6x Single Ended 3x LVDS Pairs
ADC/DAC CLK 6x Diff Clocks
6x UMCC Connectors J20, J27, J32...35, J38
PLLCLK1...7
FFA
FFB
UCC8 Connector J23
UCC8 Connector J25
FFA_SDA/SCL
FFB_SDA/SCL
I2C Switch, U7
I2C0_1V8
J18
Trenz Electronic TE0835 RFSoC
JM2
JM1
J17
UART_RX/TX
JTAG
Pin Header, J40
RESETN
Push Button, BTN1
USB
Micro USB2.0, J30
4x Lanes
Gigabit RJ45 , J31
PHY_LED0
Yellow/ Green LED
PHY_LED1
Yellow/ Green LED
CPLD_IO0...2
CPLD_JTAGEN
DIP Switch, S1
Micro SD card Connector, J28
SD Data
SDIO Expander, U11
UEC5 Connector, J22
16x Single Ended 8x LVDS Pairs
16x Single Ended 8x LVDS Pairs
UEC5 Connector, J24
DIP Switch, S2
DSPL L0_SEL0...1
16x Single Ended /8x LVDS Pairs
EXT_CLKIN_PSMGT
PCIe_RESET_N
B128_CLK1
B129_CLK1
PCIe-8x-kurz , J26
DSPL L0_LOL
Green LED, D12
CLK0
Oscillator, Y1



TEB0835 block diagram

Main Components



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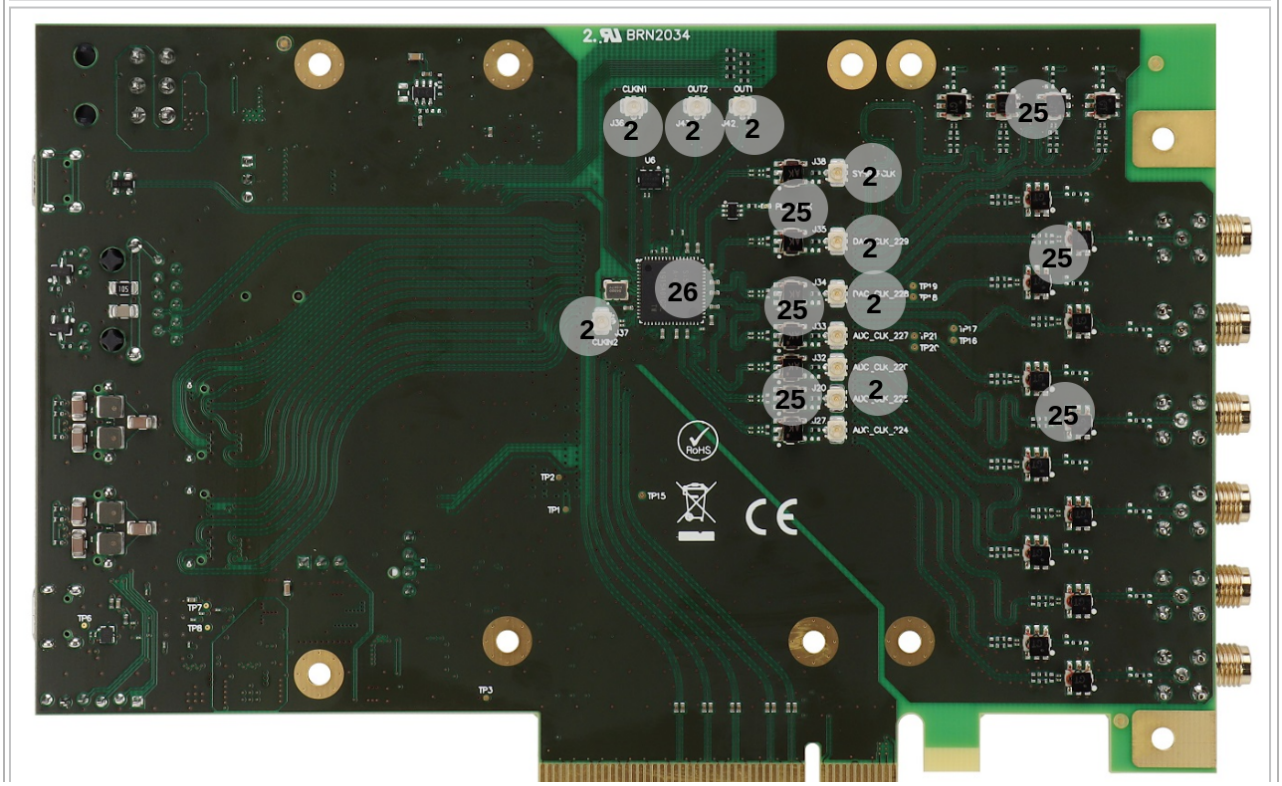

BRN2034
CLKIN1
OUT2
OUT1
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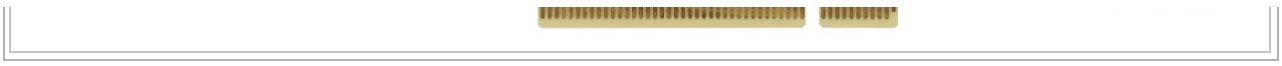
RoHS
CE



TEB0835 main components

1. SMA Connectors, J1,J3,J5,J7,J9,J11
2. UMCC Connectors, J2,J4,J6,J8, J10, J12...16, J20, J27, J32...J38, J42...43
3. Green LEDs, D6...11
4. B2B Connector, J18
5. B2B Connector, J17
6. Micro SD Card Connector, J28
7. Reset Push Button, BTN1
8. PCIe 6 Pin Connector, J19
9. Micro USB2.0 Connectors, J30
10. Gigabit RJ45 Connector, J31
11. DIP Switch, S1
12. UEC5 Connector, J22,J24
13. UCC8 Connector, J23,J25
14. 1x4 Pin Header, J21
15. FTDI, U12
16. Green LEDs, D1...3
17. 1x6 Pin Header, J40
18. Micro USB2.0 Connectors (FTDI), J29
19. PCIe-8x-kurz Card, J26
20. Battery Holder, B1
21. DIP Switch (PLL SEL), S2
22. Pin Header (PLL I2C), J41
23. Jumper (PWR CFG), J39
24. EEPROM, U15
25. RF Transformer, T2...17, T26...32
26. Programmable Clock Generator, U5

Initial Delivery State

Storage device name	Content	Notes
EEPROM	Programmed	FTDI Configuration

Initial delivery state of programmable devices on the module

Configuration Signals

Push Button BTN1 is provided to switch OFF all power supplies on RFSoC board.

Signal	B2B	I/O	Note
RESETN	J17- 36	Input	Connected to Push Button, BTN1

Reset process.

There is a DIP switch S1 provided for enabling CPLD and set the FPGA boot mode. The DIP Switch setting should be set like the following table.

DIP	Signal	Setting	Note
S1-A	CPLD_IO0	FPGA boot config	Bit 0, CPLD Firmware dependent.
S1-B	CPLD_IO1	FPGA boot config	SDA pin
S1-C	CPLD_IO2	-	PROGRAMN pin
S1-D	CPLD_JTAGEN	CPLD JTAG EN	JTAGENB

CPLD Configuration

Boot Mode must be set using DIP Switch S1 on CPLD provided on the module TE0835. Please note that the DIP Switch is active low.

MODE Signal State	Boot Mode	
	S1-A	S1-B
JTAG	ON	ON
QSPI Flash	ON	OFF
SD Card	OFF	OFF

Boot process.

Signals, Interfaces and Pins

Board to Board (B2B) I/Os

Number of I/O signals and interfaces connected to the B2B connectors:

B2B Connector	Interface	I/O Signal Count	Connected to	Notes
J17	I2C	3x Single Ended	I2C Switch, U7	
	PLL Intrupt PLL Clocks	1x Single Ended 4x Single Ended, 2x Differential pairs	PLL Clock Generator, U5	
	JTAG	4x Single Ended	FTDI, U12	
	CPLD IO CPLD Enable	3x Single Ended 1x Single Ended	DIP Switch, S1	
	PCIe Reset	1x Single Ended	PCIe Card, J26	
	UART	2x Single Ended	FTDI, U12	
	Ethernet LED Ethernet MDI	2x Single Ended 8x Single Ended	RJ45 Connector, J31	
	SD Card	6x Single Ended	Micro SD Memory Connector, J28 IO Expander, U11	
	I/O	16x Single Ended, 8x Differential pairs	PCIe Card, J26	PCIe
	I/O	16x Single Ended, 8x Differential pairs	UEC5 Connector, J22	UEC5
	I/O	16x Single Ended, 8x Differential pairs	UEC5 Connector, J24	UEC5
	Micro USB2.0	2x Single Ended 1x Single Ended 2x Single Ended	Micro USB2.0 Connector, J30 Voltage Regulator, U17 Diode, D5	

J18	ADC	16x Single Ended, 8x Differential pairs	SMA, J1, J3, J5, J7 UMCC, J2, J4, J6, J8	
	ADC Clock	4x Single Ended, 2x Differential pairs	UMCC, J27, J32	
	DAC	16x Single Ended, 8x Differential pairs	SMA, J9, J11 UMCC, J10, J12, J13...16	
	DAC Clock	4x Single Ended, 2x Differential pairs	UMCC, J33, J34	
	Green LEDs	6x Single Ended, 3x Differential pairs	Green LEDs, D6...11	
	I/O	10x Single Ended	UCC8 Connector, J23, J25	UCC8

B2B connections information

Gigabit Ethernet

Signal Name	Connected to	Signal Description	Note
PHY_MDI0...3	B2B, J17	Media Data	
PHY_LED0...1	B2B, J17	Speed/Link Indicators LED	Yellow/Green

Gigabit Ethernet information

Micro USB for JTAG/UART

The TEB0835 is equipped with two Micro USB2.0 Connectors J29, J30. The Micro USB2.0 port, J29 is provided for JTAG/UART and it is connected to FTDI, U12.

Designator	Signal Name	Connected to	Note
J29	D_N/D_P	FTDI,U12	Data
	USB_VBUS	Diode, D4	VBUS

Micro USB2 to JTAG/UART connections

Micro USB2.0

There is a Micro USB2.0 J30, provided for user.

Designator	Signal Name	Connected to	Note
J30	USB_N/USB_P	B2B, J17	Data
	USB0_VBUS	B2B, J17	VBUS
	USB0_ID	B2B, J17	ID

Micro USB2.0 Socket connections

Micro SD Card Reader

There is a Micro SD Card socket J28 connected to B2B J17 through an I/O expander U11.

Pin	Signal Name	Connected to	Note
VDD	3.3V_SD	B2B, J17	connected to IO expander
CMD	SD_CMD	B2B, J17	connected to IO expander
CLK	SD_CLK	B2B, J17	connected to IO expander
DATA0...3	SD_DATA0...3	B2B, J17	connected to IO expander
CD	SD_CD	B2B, J17	

Micro SD Card Socket connections

SMA Connectors

There are 6 SMA Connectors provided for Analog and Digital signals.

Designator	Signal Name	Connected to	Note
J1	ADC0_IN	B2B, J18	Via RF Transformer T2
J3	ADC2_IN	B2B, J18	Via RF Transformer T6
J5	ADC4_IN	B2B, J18	Via RF Transformer T4
J7	ADC6_IN	B2B, J18	Via RF Transformer T8
J9	DAC0_OUT	B2B, J18	Via RF Transformer T10
J11	DAC2_OUT	B2B, J18	Via RF Transformer T12

SMA Connectors information

UMCC Connectors

There are 21x UMCC Connectors provided for Analog /Digital signals and Clocks input and output.

Designator	Signal Name	Connected to	Note
J2	ADC1_IN	B2B, J18	Via RF Transformer T3
J4	ADC3_IN	B2B, J18	Via RF Transformer T5
J6	ADC5_IN	B2B, J18	Via RF Transformer T7
J8	ADC7_IN	B2B, J18	Via RF Transformer T9
J10	DAC1_OUT	B2B, J18	Via RF Transformer T11
J12	DAC3_OUT	B2B, J18	Via RF Transformer T13
J13	DAC4_OUT	B2B, J18	Via RF Transformer T14
J14	DAC5_OUT	B2B, J18	Via RF Transformer T15
J15	DAC6_OUT	B2B, J18	Via RF Transformer T16
J16	DAC7_OUT	B2B, J18	Via RF Transformer T17
J27	ADC_CLK_224	B2B, J18	Via RF Transformer T26
J20	ADC_CLK_225	B2B, J18	Via RF Transformer T27
J32	ADC_CLK_226	B2B, J18	Via RF Transformer T28
J33	ADC_CLK_227	B2B, J18	Via RF Transformer T29
J34	DAC_CLK_228	B2B, J18	Via RF Transformer T30

J35	DAC_CLK_229	B2B, J18	Via RF Transformer T31
J36	CLKIN1	Programmable Clock Generator, U5	
J37	CLKIN2	Programmable Clock Generator, U5	
J38	CLKOUT7	Programmable Clock Generator, U5	Via RF Transformer T32
J42	CLKOUT8	Programmable Clock Generator, U5	
J43	CLKOUT9	Programmable Clock Generator, U5	

UMCC Connectors

UCE5 Connectors

The TEB0835 is equipped with two UCE5 Connectors.

Designator	Signal Name	Connected to	Note
J22	B128_TX0...3	B2B, J17	8x Single Ended/ 4x LVDS Pairs
	B128_RX0...3	B2B, J17	8x Single Ended/ 4x LVDS Pairs
J24	B129_TX0...3	B2B, J17	8x Single Ended/ 4x LVDS Pairs
	B129_RX0...3	B2B, J17	8x Single Ended/ 4x LVDS Pairs

UEC5 Connectors

UCC8 Connectors

The TEB0835 is equipped with two UCC8 Connectors.

Designator	Signal Name	Connected to	Note
J23	FFA_MPRS	B2B, J17	
	FFA_MSEL	B2B, J17	
	FFA_INTL	B2B, J17	
	FFA_RSTL	B2B, J17	
	FFA_SCL/FFA_SDA	I2C Switch, U7	
J25	FFB_MPRS	B2B, J17	
	FFB_MSEL	B2B, J17	
	FFB_INTL	B2B, J17	
	FFB_RSTL	B2B, J17	
	FFB_SCL/FFB_SDA	I2C Switch, U7	

UCC8 Connectors

PCIe 8x Short

There is a PICe-8x-Short card provided on the TEB0835 board.

Signal Name	Connected to	Note
B505_RX0...3	B2B, J17	8x Single Ended/ 4x LVDS Pairs
B505_TX0...3	B2B, J17	8x Single Ended/ 4x LVDS Pairs
EXT_CLKIN_PSMGT	B2B, J17	
PCIE_RSTB_R	B2B, J17	Pulled up to 1.8V

PCIe x8 Kurz Connections

PCIe 6 Pins

Pin	Signal Name	Connected to	Note
1	12V_input_A	Regulator, U2	
2			
3			
4	GND	N.C	
5			
6			

PCIe 1x6 Connection

Pin Header 1x4

Pin	Signal Name	Connected to	Note
1	GND	GND	
2	FAN_PWR	12V	
3	FAN_TACH	Tepmerature Sensor, U9	
4	FAN_PWM	Tepmerature Sensor, U9	

Pin Header1x4 Connections

Pin Header 1x6

There is a 1x6 Pin Header J40, connected to JTAG signals as the following.

Pin	Signal Name	Connected to	Note
1	JTAG_TMS	B2B, J17 FTDI, U12	
2	JTAG_TDI	B2B, J17 FTDI, U12	
3	JTAG_TDO	B2B, J17 FTDI, U12	

4	JTAG_TCK	B2B, J17 FTDI, U12	
5	GND	-	
6	3.3V_MODULE	B2B, J17	

Pin Header1x6 Connections

Pin Header 1x3

There is a 1x3 Pin Header J41, it provides access to I2C signals which are connected to I2C Switch, U7.

Pin	Signal Name	Connected to	Note
1	DSPLL0_SCL	I2C Switch, U7	
2	GND	I2C Switch, U7	
3	DSPLL0_SCL	I2C Switch, U7	

Pin Header 1x3 Connectors

Jumper

There is a Jumper J39 provided for setting the DCDC_EN between two signal level as the following.

Pin	Signal Name	Connected to	Note
1	PG_5V	Regulator, U8	
2	DCDC_EN	Regulator, U1, U4	
3	MODULE_PG	B2B, J17	

Jumper Connections

I2C Addresses

Designator	I2C Address	Notes
U9	0x4C	Temperature Sensor IC
U7	0x70	I2C Switch
U5	0x68	Programmable Clock Generator

I2C addresses table

Test Points

Test Point	Signal	Connected to	Notes
TP1	5V	B2B, J17	
TP2...3	GND	GND	
TP4	ADC0_VCM	B2B, J18	
TP5	ADC1_VCM	B2B, J18	

TP6	USB_VBUS	Micro USB2.0, J29	
TP7	UART0_RX	B2B, J17	
TP8	UART0_TX	B2B, J17	
TP9	ADC2_VCM	B2B, J18	
TP10	ADC3_VCM	B2B, J18	
TP11	ADC4_VCM	B2B, J18	
TP12	ADC5_VCM	B2B, J18	
TP13	ADC6_VCM	B2B, J18	
TP14	ADC7_VCM	B2B, J18	
TP15	PSBATT	Diode, D13	
TP16	CLKE_P	-	
TP17	CLKE_N	-	
TP18	CLKF_P	-	
TP19	CLKF_N	-	
TP20	CLKD_P	-	
TP21	CLKD_N	-	

Test Points Information

On-board Peripherals

Chip/Interface	Designator	Notes
EEPROM	U15	
FTDI	U12	
Temperature Sensor	U9	
DIP Switch	S1, S2	
Push Button	BTN1	
LEDs	D1...11	
Oscillators	U16, U6	
PLL Clock Generator	U5	

On board peripherals

EEPROM

There is an EEPROM U15 provided in order to store the FTDI configuration.

Pin	Schematic	Connected to	Notes
CS	EECS	FTDI, U12	
CLK	EECLK	FTDI, U12	

DIN	EEDATA	FTDI, U12	

EEPROM information

DIP Switch

There are two DIP Switches S1, S2 provided for boot mode and manual input select of programmable clock generator. For more information please refer to Configuration Signal Section

Designator	Pin	Schematic	Connected to	Notes
S1	S1A	CPLD_IO0	B2B, J17	
	S1B	CPLD_IO1	B2B, J17	
	S1C	CPLD_IO2	B2B, J17	
	S1D	CPLD_JTAGEN	B2B, J17	
S2	S2A	DSPLL0_SEL0	Programmable clock Generator, U5	
	S2B	DSPLL0_SEL0	Programmable clock Generator, U5	

DIP Switches information

Temperature Sensor

There is a temperature sensor IC U9 provided to capture the temperature and provides an alert when cooling is needed. the temperature IC is connected to I2C bus at address 0x4C.

Pin	Schematic	Connected to	Notes
TACH	FAN_TACH	Pin Header, J21	
PWM	FAN_PWM	Pin Header, J21	
D+	DX_P	Regulator, U8	
D-	DX_N	Regulator, U8	
nALERT	ALERT_N	I2C Switch, U7	
nTCRIT	THERM_N	pulled up to 3.3V	
SMBCLK	I2C_SCL_SNS	I2C Switch, U7	
SMBDAT	I2C_SDA_SNS	I2C Switch, U7	

Temperature sensor information

FTDI

The FTDI chip U12 converts signals from USB2 to a variety of standard serial and parallel interfaces. Refer to the FTDI data sheet to get information about the capacity of the FT2232H chip. FTDI FT2232H chip is used in MPPSE mode for JTAG, 2 I/O's of Channel B are routed to B2B J17 and must be used as UART.

The configuration of FTDI FT2232H chip is pre-programmed on the EEPROM U15.

FTDI Pin	Signal Schematic Name	Connected to	Notes

ADBUS0	JTAG_TCK	B2B, J17 Pin Header, J40	JTAG interface
ADBUS1	JTAG_TDI	B2B, J17 Pin Header, J40	
ADBUS2	JTAG_TDO	B2B, J17 Pin Header, J40	
ADBUS3	JTAG_TMS	B2B, J17 Pin Header, J40	
BDBUS0	UART0_RX	B2B, J17	UART
BDBUS1	UART0_TX	B2B, J17	UART
EECS/EECLK /EEDATA	BDBUS2	EEPROM, U15	FTDI configuration
DM/DP	D_N/D_P	Micro USB2.0, J29	FTDI Input

FTDI chip interfaces and pins

Push Button

Designator	Connected to	Functionality	Note
BTN1	RESETN	General Reset	

Push Button information

LEDs

Designator	Color	Connected to	Active Level	Note
D1	Green	PG_1.8V	High	
D2	Green	PG_3.3V	High	
D3	Green	PG_5V	High	
D6...11	Green	B2B, J18	High	User LED
D12	Green	Clock Generator, U5	High	

On-board LEDs

Clock Sources

Designator	Description	Frequency	Note
U6	MEMS Oscillator	100 MHz	
U16	MEMS Oscillator	12 MHz	
Y1	Crystal Oscillator	54 MHz	
U5	Programmable Clock Generator	Variable	

Osillators

Programmable Clock Generator

There is a programmable clock generator on-board (U5) provided in order to generate variable clocks for the module. The I^2C Address is 0x68.

U5 Pin	Signal	Connected to	Direction	Note
IN0	CLKIN0	Oscillator, U6	Input	
IN1	CLKIN1	UMCC Connector, J36	Input	
IN2	CLKIN2	UMCC Connector, J37	Input	
IN3	FB	Programmable Clock Generator, U5	Input/Output	
XA/XB	CLK0_XA/XB	Oscillator, Y1	Input	
IN_SEL0...1	DSPLL0_SEL0...1	I2C Switch, U7 DIP Switch, S2	Input	
nINTR	DSPLL0_INTR_N	I2C Switch, U7	Input	
nLOL	DSPLL0_LOL_N	Green LED, D12	Input	
nRST	DSPLL0_RST_N	1.8 V	Input	
SCLK	DSPLL0_SCL	I2C Switch, U7	Input	
SDA /SDIO	DSPLL0_SDA	I2C Switch, U7 Pin Header, J41	In/Out	
INTR	PLL_INTR_N	B2B, J17	Output	
OUT0A	CLKOUT0A	B2B, J17	Output	
OUT0	CLKOUT0_P	B2B, J17	Output	
OUT1	PLLCLK1	UMMC, J27	Output	
OUT2	PLLCLK2	UMMC, J20	Output	
OUT3	PLLCLK3	UMMC, J32	Output	
OUT4	PLLCLK4	UMMC, J33	Output	
OUT5	PLLCLK5	UMMC, J34	Output	
OUT6	PLLCLK6	UMMC, J35	Output	
OUT7	CLKOUT7	UMMC, J38	Output	
OUT8	CLKOUT8	UMMC, J42	Output	
OUT9	CLKOUT9	UMMC, J43	Output	
OUT9A	CLKOUT9A	Programmable Clock Generator, U5	Output	

Programmable Clock Generator Inputs and Outputs

Power and Power-On Sequence

Power Supply

Power supply with minimum current capability of 3 A for system startup is recommended.

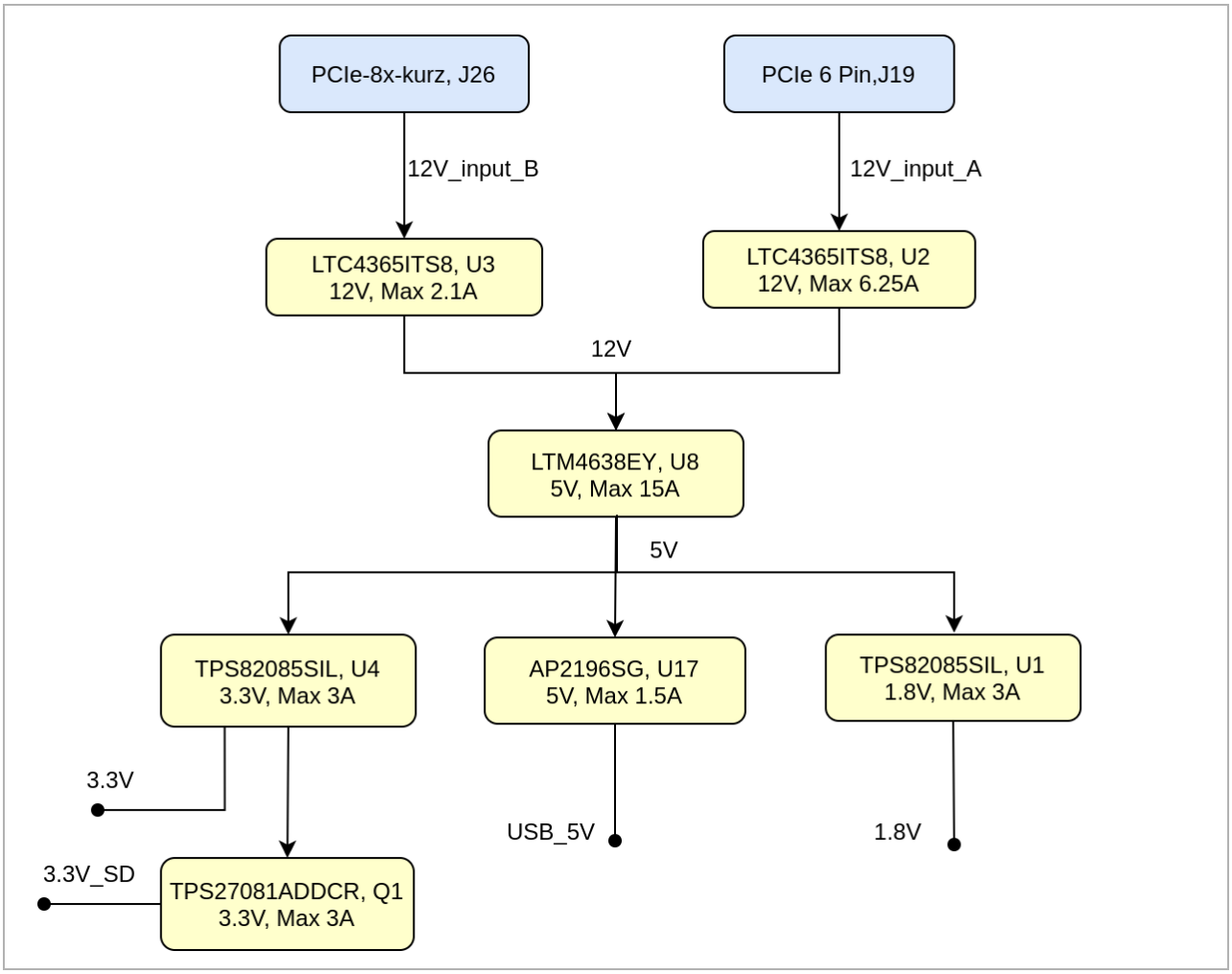
Power Consumption

Power Input Pin	Typical Current
VIN	TBD*

Power Consumption

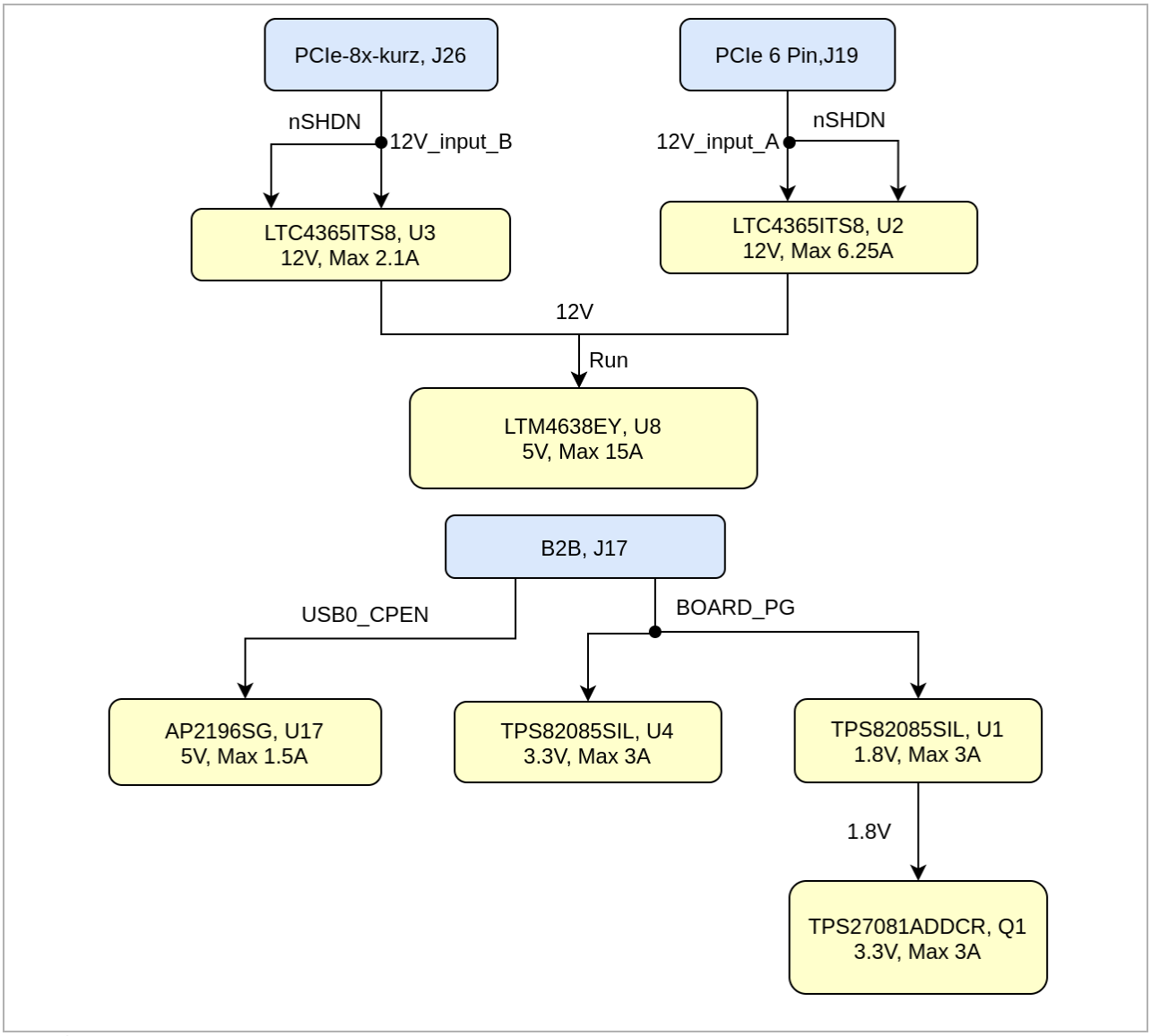
* TBD - To Be Determined

Power Distribution Dependencies



Power Distribution

Power-On Sequence



Power Sequency

Power Rails

Power Rail Name	B2B JM17	B2B JM2	Direction	Notes
5V	1,2,3,4,5,6,8	-	Ouput	
PSBATT	14	-	Output	
3.3V_MODULE	16	-	Input	

Module power rails.

Board to Board Connectors

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Technical Specifications

Absolute Maximum Ratings

Symbols	Description	Min	Max	Unit
VIN	Input Supply Voltage	2.5	34	V
ADC_V	Analog input voltage	-5.0	5.0	V
DAC_V	Digital input voltage	-5.0	5.0	°C
T_STG	Storage Temperature	-55	125	°C

PS absolute maximum ratings

Recommended Operating Conditions

Operating temperature range depends also on customer design and cooling solution. Please contact us for options.

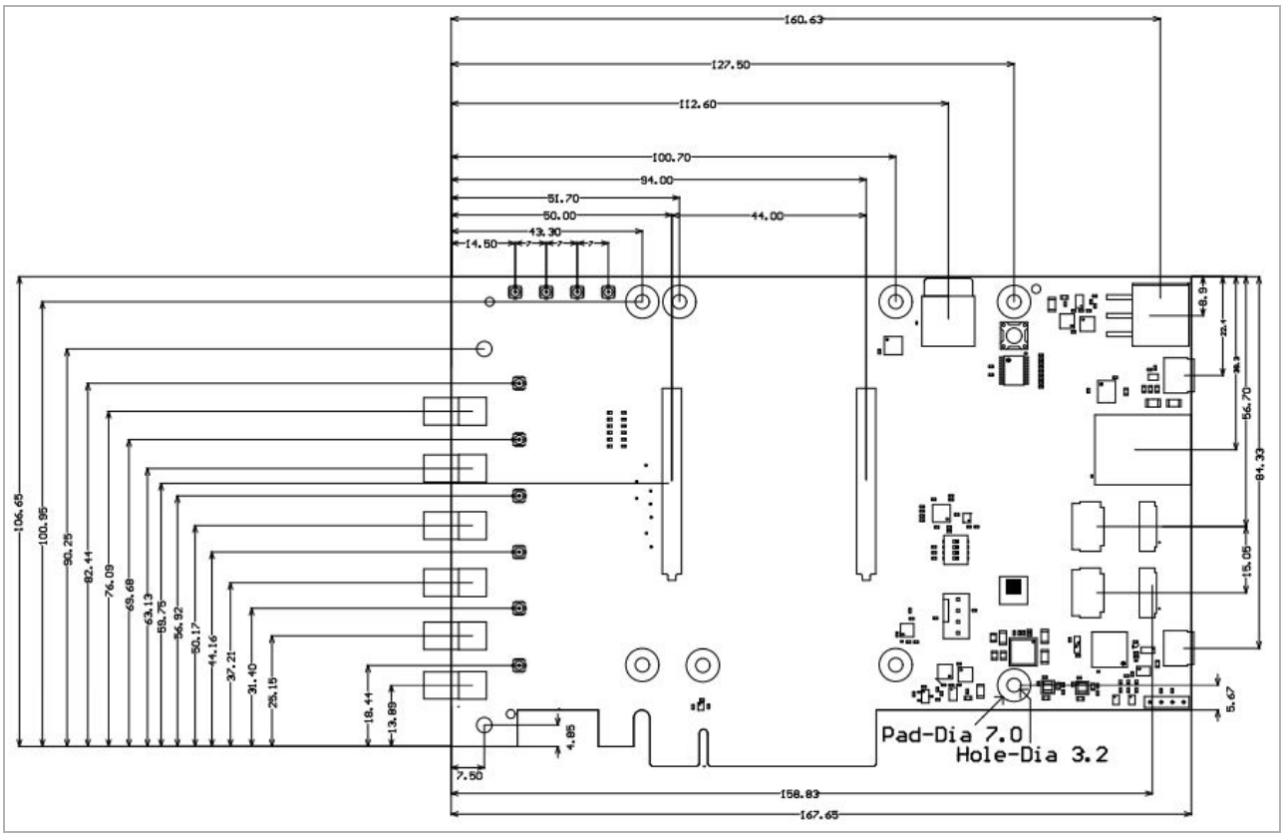
Parameter	Min	Max	Units	Reference Document
VIN	11	13	V	See the datasheet.
ADC_V	0	5	V	See the SMA datasheet
DAC_V	0	5	V	See the UMCC datasheet
T_OPT	-40	+85	°C	See RF Transformer datasheet.

Recommended operating conditions.

Physical Dimensions

- Module size: 106.6 mm × 167.7 mm. Please download the assembly diagram for exact numbers.
- Mating height with standard connectors: 5 mm.

PCB thickness: 1.5 mm.



Physical Dimension

Currently Offered Variants

Trenz shop TEB0835 overview page	
English page	German page

Trenz Electronic Shop Overview

Revision History

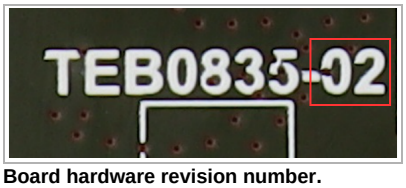
Hardware Revision History

Date	Revision	Changes	Documentation Link
2019-11-29	REV01	Initial Release	REV01

2020-08-13	REV02	1. All module's mount holes are connected to GND; 2. CLK_Connectors. Added baluns for each clock inputs; 3. Internal DSPLL is changed on SI5395A-A-GM; 4. Added ability to use internal DSPLL as a source for each clock; 5. Added clock inputs CLKIN1, CLKIN2 and clock outputs OUT1 , OUT2 connected to DSPLL.; 6. All clock traces are matched with tolerance 0.2 mm; 7. Lengths of inputs ADC0, ADC2, ADC4, ADC6 are matched with tolerance 0.2 mm; 8. Lengths of outputs DAC0 and DAC2 are matched with tolerance 0.2 mm; 9. Lengths of outputs DAC4, DAC5, DAC6, DAC7 are matched with tolerance 0.2 mm; 10. In REV02: FTDI is powered from 3.3 V_Module; 11. Signal PLL_INTR_N is removed; 12. Signal BOARD_PG is renamed in MODULE_PG; 13. Added ability to select enable signal for internal DC-DCs 3.3V and 1.8V. 14. Added JTAG connector J40. 15. Added VBAT schematic. Added a holder for CR1220 3V battery	REV02

Hardware Revision History

Hardware revision number can be found on the PCB board together with the module model number separated by the dash.



Board hardware revision number.

Document Change History

Date	Revision	Contributor	Description
Error rendering macro 'page-info' Ambiguous method overloading for method jdk.proxy279.$Proxy4022#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.	**Error rendering macro 'page-info'** Ambiguous method overloading for method jdk.proxy279.$Proxy4022#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.	**Error rendering macro 'page-info'** Ambiguous method overloading for method jdk.proxy279.$Proxy4022#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.	• update download link

atlassian . confluence. pages. Page] due to overlapping prototypes between : [interface com. atlassian . confluence.user. ConfluenceUser , class java. lang. String, class com. atlassian . confluence.core. ContentEntityObject] [interface com. atlassian .user. User,

atlassian . confluence. pages. Page] due to overlapping prototypes between : [interface com. atlassian . confluence.user. ConfluenceUser , class java. lang. String, class com. atlassian . confluence.core. ContentEntityObject] [interface com. atlassian .user. User,

atlassian . confluence. pages. Page] due to overlapping prototypes between : [interface com. atlassian . confluence.user. ConfluenceUser , class java. lang. String, class com. atlassian . confluence.core. ContentEntityObject] [interface com. atlassian .user. User,

class java. lang. String, class com. atlassian . confluen ce.core. Content EntityOb ject]	class java. lang. String, class com. atlassian . confluen ce.core. Content EntityOb ject]	class java. lang. String, class com. atlassian . confluen ce.core. Content EntityOb ject]	
2023-01-17	v.54	Kerstin Möller	• Style update
2020-12-21	v.51	Pedram Babakhani	• Update to Revision 02
--	all	**Error renderi ng macro 'page-info'** Ambiguo us method overload ing for method jdk. proxy27 9.$Proxy 4022#ha sConten	• --

tLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.

		lang. String, class com. atlassian . confluen ce.core. Content EntityOb ject] [interfac e com. atlassian .user. User, class java. lang. String, class com. atlassian . confluen ce.core. Content EntityOb ject]	

Document change history.

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Error rendering macro 'page-info'

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