

AMD Answer Record

Relevant for newer designs:

Number/Link	Description	Note
lwIP modifications for Marvell PHY	lwIP modifications This project uses a modified version of the lwIP library in order for it to work with the Marvel 88E1510/88E1518 PHYs on the Ethernet FMC. A function is added to xaxiemacif_physpeed.c for the initialization of the Marvell 88E1510 Ethernet PHY	Patch to use Marvel phy
AR#34290	Workaround for the case when running Vivado 2022.2 on newer Linux distributions and the Block Design hangs the complete UI. This is expected to be fixed in future versions.	
AR# 55854	Vivado - What can I do to resolve a Vivado crash, exception, or abnormal program termination?	
AR#72992	Design Advisory for Zynq UltraScale+ MPSoC/RFSoc: Possible link training failures or data errors on PCIe, SATA, or USB 3.0 protocol links using PS GTR	Important for Designs up to 19.2 and for SATA Gen1 also newer Vivado
AR# 68671	Zynq UltraScale+ MPSoC DisplayPort Controller - What devices are supported with the DisplayPort Controller?	
AR# 43989	7 Series FPGAs - LVDS_33, LVDS_25, LVDS_18, LVDS inputs & outputs for High Range (HR) and High Performance (HP) I/O banks	
AR# 69269	Zynq UltraScale+ MPSoC, SDK - Debugging FSBL application does not show source code	
AR# 65467	Zynq UltraScale+ MPSoC - Boot and Configuration	
AR# 66846	Method to boot from SD or eMMC from QSPI	
AR# 37347	7 Series FPGAs - Will driving the I/Os of an unpowered bank cause damage to the part? Do 7 Series devices support hot swap?	
AR# 50802	7 Series - What state are the I/Os in at power up?	
AR# 45985	7 Series - How do you limit reverse biasing of VCCO when input is being driven by a 3.3V signal before Vcco is powered?	
AR# 47317	Zynq-7000 SoC, ID - Incorrect PS Family IDCODE Value	
AR# 47916	Zynq-7000 SoC Devices - Silicon Revision Differences	
AR# 59476	Zynq-7000 SoC: SD Programming/Bootling Checklist	
AR# 70712	Zynq UltraScale+ MPSoC: PL Masters cannot access high DDR address ranges	changed with 18.3 -automatically activated
AR# 66779	Zynq UltraScale+ MPSoC: List of tested SD cards	
AR# 57744	Design Advisory for Zynq-7000 SoC - Zynq and QSPI reset requirements when using larger than 16MB flash	Trenz Wiki notes: SPI 32 Bit Addressing
AR# 55854	Vivado - What can I do to resolve a Vivado crash, exception, or abnormal program termination?	

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AR# 68449	2016.4 PetaLinux: Migrating U-boot configs from 2016.3 PetaLinux project to 2016.4 PetaLinux Yocto based project	
AR# 68446	2016.4 PetaLinux: Migrating Kernel configs from 2016.3 PetaLinux project to 2016.4 PetaLinux Yocto based project	
AR# 68440	2016.4 PetaLinux: Migrating Applications from 2016.3 PetaLinux project to 2016.4 PetaLinux Yocto based project	
AR# 66652	Zynq UltraScale+ MPSoC ZCU102 Evaluation Kit - Base TRD Monitor requirements	
AR# 68006	Design Advisory for Xilinx Design Tools (Vivado, SDAccel, SDSoc) 2016.1 and 2016.2 write_bitstream - Multi-threading might cause configuration memory cells to be set incorrectly	