# **CR00140 Motor kit getting started**

Develop, simulate and test of motor control algorithms with this modular motor kit is supported by MathWorks with hardware support packages for Matlab and Simulink (licence needed).

- Content of the kit
- Preparation of CR00140 kit
- Preparation for test of CR00140 with Motor
- Preparation of Software
- Motor test

# Content of the kit

The motor kit is available in two configurations with either a Zynq Ultrascale+ SoM (TE0820 in Kit CR00140-02-K0), or 7 series Zynq SoM (TE0720-03-1CFA in Kit CR00140-02-K1). The parts of the Motorkit are listed in the following table. The main components are linked to their general resources pages where detailed information like TRMs, schematic, firmware and firmeware description, assembly diagramms can be found.

For further insights see also the TRMs of each specific component:

- TE0820 TRM or TE0720 TRM
- TEB0707 TRM
- CR00140 TRM

Components	Article number	Description
TEB0707	TEB0707-02	baseboard
CR00140	CR00140-02	motor driver board
TE0820 (option K0) or TE0720 (option K1)         TE0820-03-2AE21FA or TE0720-03-1CFA		SoM
BLY172D-24V-4000-1250SI	30430	motor with encoder
Included Accessories		
micro SD Card	26507	8GB SDHC
heat sink	28606 or 26922	(type depends on module) with assebly material (pre assembled)
5V power supply	28485	for baseboard (barrel plug)
encoder cable	TEC0140-01-C	

Additional accessories needed, not included:

Components	Description	
24V power supply	with cables suitable for screw terminals	
Ethernet cable	connection to development PC	
micro USB cable	connection to development PC	

### Preparation of CR00140 kit

Compare with picture below.

- 1. Place FPGA Module (TE0820 or TE0720) with cooler on TEB0707
- 2. Place CR00140 on TEB0707
- 3. Jumper and Dip setting
  - a. Jumper setting on TEB0707: J4: TE0820: ŠD3.3V; TE0720: SD->1.8V J5: CA IOV,
    - J6: CB IOV,
    - J7: CC IOV
  - b. Dips on TEB0707: S1-1..4 all "OFF"
  - c. CR00140 Jumper configuration for single ended encoder J3: 1-2, 5-6, 9-10

With TE0720



With TE0820

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# Preparation for test of CR00140 with Motor

Compare with picture in section 'Motor test - 3.' below.

- 1. Connect 5V DC adapter to TEB0707 (J1)
- Connect Ethernet of TEB0707 (J2) (direct connection to PC, e.g. USB-ETH Adapter)
   Connect micro USB of TEB0707 (J15) to PC (Not needed for Test, but for debugging UART serial console)
- 4. Connect Motor phases (J8 screw terminal)
  - a. yellow A b. red B



- Connect 24V on CR00140 (J7 screw terminal). Check polarity!
   Connect motor-encoder via 5-pin encoder cable to J1 of CR00140. On both sides (Motor and CR00140) the brown wire is connected to pin 1.

#### **Preparation of Software**

Correct Vivado and MatLAB versions corresponding to the Mathworks motor control design are needed.

- 1. Copy all data of the corresponding Mathworks Motor control SD-image for TE0820 or TE0720 onto a SD-Card.
- 2. Place the SD-Card into TEB0707 (J8)
- 3. Open Matlab a.

check	check that following two AddOns are installed in actual version				
	HDL Coder Support Package for Xilinx Zynq Platform version 20.2.2	✦ Hardware Support Package	7 December 2020	@ :	Ì
	Embedded Coder Support Package for Xilinx Zyng Platform version 20.2.1	📣 Hardware Support Package	7 December 2020	@ :	

- b. check package setup for both packages (available via Matlab Home Add-Ons AddManage Add-Ons grey gear)
  - i. Select Hardware Board

TE0720	TE0820
Xilinx Zynq ZC702 evaluation kit	Xilinx Zynq ultraScale+ MPSoC ZCU102 Evaluation kit



use option "Connect directly to development computer"

- Set IP Address to 192.168.1.X (SoC has 192.168.1.101)
- c. register vivado version 20XX.X adding in file "~\Documents\MATLAB\startup.m": hdlsetuptoolpath('ToolName','Xilinx Vivado', 'ToolPath', 'C:\Xilinx\Vivado\20XX.X\bin\vivado.bat')
- if other directory is used for installation it has to be changed accordingly, replace X by used version of Mathworks design.
- 4. Open Mathworks motor control demo project for TE0820 or TE0720

- a. Ignore warning about path Work does not exist: OKContinue b. open t4\_open hdlWorkflowadvisor

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c. select under 1.1 "Target platform" correct board:

Trenz TE0720	with CR00140	Trenz TE0820 with CR00140	
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	For more information, right-click a task and select "What's Thic?".  For a fat of all possible actions, right-click an item in the Task Herandry. Lugend  A Running bits check triggers an update Degram.  A Running bits check triggers an extension analysis.

- e. Do same (run all) for 2., 3.1, 3.2 (needs some time, press ok if window opens, will close automatically when finished) f. run all tasks excluding 4.4
  - i. 4.3 will need approx 10 minutes on an up to date desktop PC.

Auswählen C:\Windows\SYSTEM32\cmd.exe	-		×
INFO: [Project 1-570] Preparing netlist for logic optimization INFO: [Timing 38-478] Restoring timing data restore complete. INFO: [Timing 38-479] Binary timing data restore complete. INFO: [Project 1-856] Restoring constraints from binary archive. INFO: [Project 1-853] Binary constraint restore complete. Reading XDEF placement. Reading XDEF routing. Read XDEF File: Time (s): cpu = 00:00:03 ; elapsed = 00:00:03 . Memory (MB): peak = 1765.324 ; gain = 36.5 Restored from archive   CPU: 3.000000 secs   Memory: 0.000000 MB   Finished XDEF File Restore: Time (s): cpu = 00:00:03 ; elapsed = 00:00:03 . Memory (MB): peak = 1765.324 ; gain = 36.5	324 gain	ı = 36.	824
Netlist sorting complete. Time (S): cpu = 00:000; elapsed = 00:00:00.004 . Memory (MB): peak = 1765.324 0 INFO: [Project 1-111] Unisim Transformation Summary: A total of 41 instances were transformed. DSP48E2 = > DSP48E2 (DSP_ALU, DSP_A_B_DATA, DSP_C_DATA, DSP_MULTIPLIER, DSP_M_DATA, DSP_OUTPUT, DSP_PREAL EADD): 29 instances IBUF => IBUF (IBUFCTRL, INBUF): 5 instances RAM32MI6 => RAM32M16 (RAMD32, RAMD32, RAMD3	DD_DAT	A, DSP RAMD3	.00 _pr 2,
open_run: Time (s): cpu = 00:00:26 ; elapsed = 00:00:29 . Memory (MB): peak = 1765.324 ; gain = 1136.500 get_timing_paths: Time (s): cpu = 00:00:12 ; elapsed = 00:00:10 . Memory (MB): peak = 2287.930 ; gain = 52 	2.605		
INFO: [Common 17-206] Exiting Vivado at Fri Dec 11 12:40:41 2020 C:\Users\test-cr00140\Desktop\CR00140-TE0720\pmsmfoc R2020b dec021\Work\hdl pri\vivado ip pri>			

ii. close all Matlab windows and project (and save if asked)

#### **Motor test**

- 1. Power on TBE0707 (5V)

  - a. check current: ~1.0A b. check shortly after start Done LED goes of

TE0720	TE0820	
green LED D4	red LED D1	

- c. 3 red LEDs on TEB0707 go off after Linux startup. This indicates system ready for test.
  2. Power on CR00140 motor stage (24V)

a. check current ~0.05Å

3. Press push button S1 on CR00140 (D1 on CR00140 should now blink) The setup should look like this, (+cooler on Module)



- 4. Open saved Matlab project from above.
- 5. t6\_download Bitstream (module will automatically restart, no vivado HW manger should be connected, otherwise restart will fail.)



#### a. Current consumption

TE0720	TE0820
~0.8 A	~1.2 A

- b. three red LEDs D4, D5, D6 on TEB0707 go off after peatlinux is up completely. (Can also be checked via UART console, e.g. use putty, Baut rate 115200)
- 6. open t7\_openZynqARMmodel
  - a. If Scope window doesen't open automatically, double click on Scope
  - b. Press Run

c. Wait until motor demo has finished (1 minute +)



