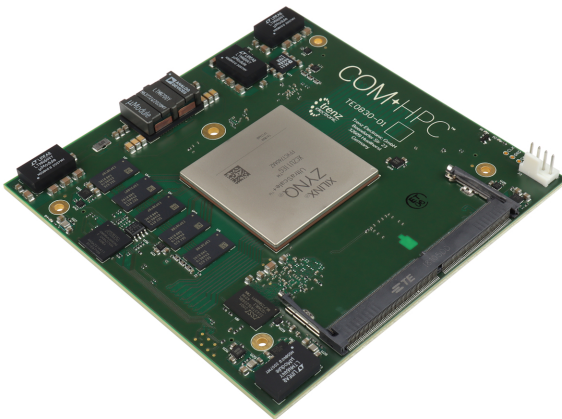


TE0830



Expected release in Q2 2025

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Key Features

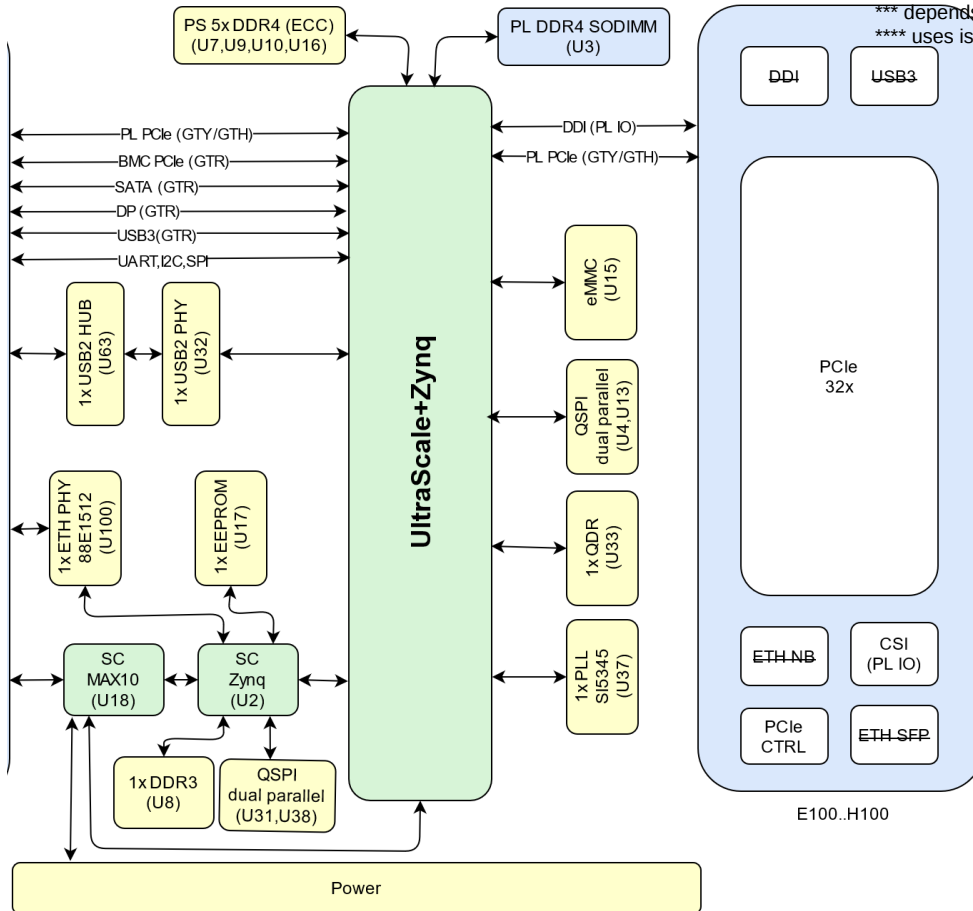
- **SoC/FPGA (UltraScale+ Zynq)**
 - Package: FFVC1760
 - Device: ZU11, ZU17, ZU19*
 - Engine: EG
 - Speed: -1, -2, -3*, **
 - Temperature: I, E, (Q, M)*, **
- **RAM/Storage**
 - DDR4 (PS connected)
 - Data width: 72bit with ECC
 - Size: def. 4GB (up to 8GB possible)*
 - Speed:***
 - DDR4 SODIMM (PL connected)
 - 72-Bit DDR4 with ECC
 - Size: max 16GB*
 - Speed: NA*
 - eMMC
 - Data width: 8Bit
 - size: def. 8GB (up to 64 possible)*
 - QSPI boot Flash in dual parallel mode (size depends on assembly version)
 - Data width: 8bit
 - size: def. 128MB (up to 512MB possible)*
 - QDDRII (optional, default not assembled)
 - size:18Mbit*
 - MAC address serial EEPROM with EUI-48™ node identity (Microchip 24AA025E48)
- **On Board**
 - SC CPLD and SoC
 - MAX10: 10M08
 - 7 Series Zynq: XC7Z010 with 128MB QSPI and 512MB DDR3 (16Bit)
 - PLL SI5345
 - Gigabit ETH PHY (Marvell Alaska 88E1512)
 - USB2 HUB
 - USB2 PHY
- **Interface (2 x 400pin COM-HPC connectors)**
 - PCIe SMB 1x (ZynqMP PS GTR)
 - PCIe up to 48 lane (16x GTY(32.75 Gb/s) and 32x GTH (16.3 Gb/s))****
 - Gbit Ethernet 1x
 - USB2 4x
 - USB3 1x (ZynqMP PS GTR)
 - DDI (DP) 1x (ZynqMP PS GTR)
 - SATA 1x (ZynqMP PS GTR)
 - SPI 1x
 - I2C SMB 1x
 - I2C 3x
 - UART 2x (1x ZynqMP, 1x SC Zynq)
 - GPIO 12x (JTAG over GPIO)
 - PL HP IOs x32 (15 diff) over COM-HPC CSI Interface
- **Power**
 - 12V Main
 - 5V Standby
 - 2.0-3.3V RTC

• **Dimension**

COM-HPC Client module Size B (120x120mm)

Notes

- * depends on assembly version
- E1..H1 ** not all combinations are possible
- *** depends on used U+ Zynq and DDR4 combination
- **** uses is limited by U+ Zynq specification



E100..H100