TEB0912 CPLD

Overview

Lattice MachXO2-4000HC is a CPLD chip, that is used in TEB0912 board as a system management controller. The system controller implements power management same as power sequencing, . Rather than power management is, the system controller responsible for reset generation, zynq initial configuration. System controller contains of some additional features same as debouncing the power button and displaying the power status with LEDs. The JTAG and UART interfaces are routed in the firmware of CPLD from FTDI chip to FPGA. In this board the CPLD is responsible for controlling and monitoring of power supply of the board, There are various DC-DC converter or regulators , one input current sensor and six temperature sensors. To control every converter chip or regualtor monitors CPLD power good outputs of regulators or DC-DC converters continuously to avoid over-voltage in the power system. System controller reads the measured temperature of all temperature sonsors continuously to avoid over-temperature in regulators or DC-DC converter chips. The firmware of CPLD contains of various subsystems same as I2c master and I2c slave subsystems. I2c master reads the data of current sensor and 6 temperature sensors , that measure the temperature of DC-DC converter chips. I2c slave is responsible for communicating with FPGA to read register addresses and write the measured data in FPGA.

Feature Summary

- Power Management
- Reset Management
- JTAG Routing
- Boot Mode
- User IOs
- LED and power state display
- UART
- I2C Slave
- I2C Master
- I2C to GPIO
- RAM Memory
- Data Management State Machine
- Temperature Sensor TMP461
- Current Sensor INA219AIDCNR

Firmware Revision and supported PCB Revision

See Document Change History

Product Specification

Port Description

Name / opt. VHDL Name	Direction	Pin	Pullup/Down (HW)	Bank Power	Description

ALERT_N	in	B33	--- (UP)	+3.3V_STB	Digital output . Interrupt or SMBus alert output of temperature sensors (TMP461AIRUNT- U43,U47,U52, U57,U4) and temperature sensor with integrated fan control (LM96163-U61) / currently_not_used
CPLD_DEBUG0	inout	A41	NONE (UP)	+3.3V_STB	CPLD debug pin 0
CPLD_DEBUG1	inout	A2	UP (UP)	+3.3V_STB	CPLD debug pin 1 -- For monitoring of I2C master clock (SCL)
CPLD_DEBUG2	inout	B1	UP (UP)	+3.3V_STB	CPLD debug pin 2 -- For monitoring of I2C master data (SDA)
CPLD_DEBUG3	inout	A3	--- (NONE)	+3.3V_STB	CPLD debug pin 3 /currently_not_used
CPLD_HD0	inout	B3	UP (UP)	+3.3V_STB	High density IOs select 0
CPLD_HD1	inout	B28	UP (UP)	+3.3V_STB	High density IOs select 1
EN_VCCINT	out	B22	NONE (DOWN)	+3.3V_STB	Enable pin for +0.85V DC-DC converter (LTM4630EY-U42A)
EN_VTT_DDR	out	A22	NONE (DOWN)	+3.3V_STB	Enable pin for 2A Peak Sink /Source DDR Termination Regulator (TPS51206-U2, U3)
EN+0.85V_GT_AVCC_PS/ EN_0V85_GT_AVCC_PS	out	B21	NONE (DOWN)	+3.3V_STB	Enable pin for 1.5A low-dropout linear regulator (TPS74801DRC-U45)
EN+0.9V_GT_AVCC/ EN_0V9_GT_AVCC	out	B14	NONE (DOWN)	+3.3V_STB	Enable pin for quad DC-DC microModule regulator with configurable 4A output array for +0.9V output voltage (LTM4644EY-U44)

EN+1.0V/ EN_1V0	out	A46	NONE (DOWN)	+3.3V_STB	Enable pin for 1.5A low-dropout linear regulator with +1.0V output voltage (TPS74801DRC-U13)
EN+1.2V_DDR/ EN_1V2_DDR	out	A34	NONE (DOWN)	+3.3V_STB	Enable pin for quad DC-DC microModule regulator with configurable 4A output array for +1.2V output voltage (LTM4644EY-U53)
EN+1. 2V_GT_AVTT/ EN_1V2_GT_AVTT	out	B16	NONE (DOWN)	+3.3V_STB	Enable pin for quad DC-DC microModule regulator with configurable 4A output array for +1.2V output voltage (LTM4644EY-U48)
EN+1. 2V_PLL_PS/ EN_1V2_PLL_PS	out	A15	NONE (DOWN)	+3.3V_STB	Enable pin for 1.5A low-dropout linear regulator (TPS74801DRC-U46)
EN+1. 3V_MGT_PS/ EN_1V3_GT_PS	out	B15	NONE (DOWN)	+3.3V_STB	Enable pin for quad DC-DC microModule regulator with configurable 4A output array for +1.37V output voltage (LTM4644EY-U44)
EN+1.8V/ EN_1V8	out	B13	NONE (DOWN)	+3.3V_STB	Enable pin for quad DC-DC microModule regulator with configurable 4A output array for +1.8V output voltage (LTM4644EY-U53)
EN+1.8V_AUX/ EN_1V8_AUX	out	A30	NONE (DOWN)	+3.3V_STB	Enable pin for 1.5A low-dropout linear regulator with +1.8V output voltage (TPS74801DRC-U49, U50,U51)
EN+1. 8V_GT_AVTT_PS/ EN_1V8_GT_AVTT_PS	out	B20	NONE (DOWN)	+3.3V_STB	Enable pin for 1.5A low-dropout linear regulator with +1.8V output voltage (TPS74801DRC-U54)

EN+2.5V_DDR/ EN_2V5_DDR	out	A44	NONE (DOWN)	+3.3V_STB	Enable pin for 1.5A low-dropout linear regulator with +2.5V output voltage (TPS74801DRC-U55, U56)
EN+2V_MGT_PS/ EN_2V0_GT_PS	out	A21	NONE (DOWN)	+3.3V_STB	Enable pin for quad DC-DC microModule regulator with configurable 4A output array for +2.0V output voltage (LTM4644EY-U48)
EN+3.3V/ EN_3V3	out	B18	NONE (DOWN)	+3.3V_STB	Enable pin for quad DC-DC microModule regulator with configurable 4A output array for +3.3V output voltage (LTM4644EY-U1)
EN+5V_BIAS/ EN_5V_VBIAS	out	A17	NONE (DOWN)	+3.3V_STB	Enable pin for low dropout linear regulator with +5V output voltage (ADP7102ACPZ-U58)
EXT_STATUS_LED_G	out	B9	--- (NONE)	+3.3V_STB	External status LED green (J40-Pin2) /currently_not_used
EXT_STATUS_LED_R	out	A25	--- (NONE)	+3.3V_STB	External status LED red (J40-Pin3) /currently_not_used
FAN_EN	out	B29	NONE (UP)	+3.3V_STB	Enables a smart high-side power switch to drive the FAN (BTS41411N-U60)
FPGA_DONE	in	A24	NONE (UP)	+3.3V_STB	FPGA PL configuration done indicator
FTDI_PWR_EN_N	in	A36	NONE (UP)	+3.3V_STB	Active low power enable output of FTDI chip (FT2232H56Q-U38)
FTDI_RX	out	A35	NONE (NONE)	+3.3V_STB	UART RXD of FTDI chip (FT2232H56Q-U38)
FTDI_TCK	in	A45	UP (NONE)	+3.3V_STB	FTDI JTAG clock pin (FT2232H56Q-U38)

FTDI_TDI	in	A47	UP (NONE)	+3.3V_STB	FTDI JTAG data input pin (FT2232H56Q-U38)
FTDI_TDO	out	A48	NONE (NONE)	+3.3V_STB	FTDI JTAG data output pin (FT2232H56Q-U38)
FTDI_TMS	in	B34	NONE (NONE)	+3.3V_STB	FTDI JTAG mode select pin (FT2232H56Q-U38)
FTDI_TX	in	B27	UP (NONE)	+3.3V_STB	UART TXD of FTDI chip (FT2232H56Q-U38)
I2C_SCL_CPLD	inout	B32	NONE (UP)	+3.3V_STB	I2C clock pin that connected to all temperature sensors and current sensor
I2C_SDA_CPLD	inout	A42	NONE (UP)	+3.3V_STB	I2C data pin that connected to all temperature sensors and current sensor
JTAGEN	in	B30	--- (DOWN)	+3.3V_STB	JTAG enable input pin of CPLD (Dip switch S4-1) If logical low, JTAG routed to FPGA. If logical high, CPLD access.
MIO30 / MIO30_UART0_RXD	out	A8	NONE (NONE)	+1.8V	MIO30 pin of FPGA (XCZU11EG-1FFVC1760I-U30R)
MIO31 /MIO31_UART0_TXD	in	A9	UP (NONE)	+1.8V	MIO31 pin of FPGA (XCZU11EG-1FFVC1760I-U30R)
MIO32 / MIO32_UART1_TXD	in	B8	--- (NONE)	+1.8V	MIO32 pin of FPGA (XCZU11EG-1FFVC1760I-U30R) /currently_not_used
MIO33 / MIO33_UART1_RXD	out	B7	--- (NONE)	+1.8V	MIO33 pin of FPGA (XCZU11EG-1FFVC1760I-U30R) /currently_not_used

MR	out	A26	UP (UP)	+3.3V_STB	Manual-reset that connected to MR pin of ultralow supply-current voltage monitor chip (TPS3106K33DBVR-U73)
NetU68_B2		B2	---		/currently_not_used
PG_VCCINT	in	B23	NONE (UP)	+3.3V_STB	Power good pin for +0.85V DC-DC converter (LTM4630EY-U42A)
PG+0.85V_GT_AVCC_PS/ PG_0V85_GT_AVCC_PS	in	B12	NONE (UP)	+3.3V_STB	Power good pin for 1.5A low-dropout linear regulator for +0.85V output voltage (TPS74801DRC-U45)
PG+0.9V_GT_AVCC/ PG_0V9_GT_AVCC	in	A18	NONE (UP)	+3.3V_STB	Power good pin for quad DC-DC microModule regulator with configurable 4A output array for +0.9V output voltage (LTM4644EY-U44)
PG+1.0V/ PG_1V0	in	B35	NONE (UP)	+3.3V_STB	Power good pin for 1.5A low-dropout linear regulator with +1.0V output voltage (TPS74801DRC-U13)
PG+1.2V_DDR/ PG_1V2_DDR	in	A33	NONE (UP)	+3.3V_STB	Power good pin for quad DC-DC microModule regulator with configurable 4A output array for +1.2V output voltage (LTM4644EY-U53)
PG+1.2V_GT_AVTT/ PG_1V2_GT_AVTT	in	A11	NONE (UP)	+3.3V_STB	Power good pin for quad DC-DC microModule regulator with configurable 4A output array for +1.2V output voltage (LTM4644EY-U48)

PG+1.2V_PLL_PS/ PG_1V2_PLL_PS	in	A28	NONE (UP)	+3.3V_STB	Power good pin for 1.5A low-dropout linear regulator for +1.2V output voltage (TPS74801DRC-U46)
PG+1.3V_MGT_PS/ PG_1V3_MGT_PS	in	A20	NONE (UP)	+3.3V_STB	Power good pin for quad DC-DC microModule regulator with configurable 4A output array for +0.9V output voltage (LTM4644EY-U44)
PG+1.8V/ PG_1V8	in	B25	NONE (UP)	+3.3V_STB	Power good pin for quad DC-DC microModule regulator with configurable 4A output array for +1.8V output voltage (LTM4644EY-U53)
PG+1.8V_AUX/ PG_1V8_AUX	in	A27	NONE (UP)	+3.3V_STB	Power good pin for 1.5A low-dropout linear regulator with +1.8V output voltage (TPS74801DRC-U50)
PG+1.8V_AUX_PS/ PG_1V8_AUX_PS	in	B10	NONE (UP)	+3.3V_STB	Power good pin for 1.5A low-dropout linear regulator with +1.8V output voltage (TPS74801DRC-U51)
PG+1.8V_GT_AUX/ PG_1V8_GT_AUX	in	A13	NONE (UP)	+3.3V_STB	Power good pin for 1.5A low-dropout linear regulator with +1.8V output voltage (TPS74801DRC-U49)
PG+1.8V_GT_AVTT_PS/ PG_1V8_GT_AVTT_PS	in	A16	NONE (UP)	+3.3V_STB	Power good pin for 1.5A low-dropout linear regulator with +1.8V output voltage (TPS74801DRC-U54)
PG+2.5V_DDR/ PG_2V5_DDR	in	A32	NONE (UP)	+3.3V_STB	Power good pin for 1.5A low-dropout linear regulator with +2.5V output voltage (TPS74801DRC-U55)

PG+2.5V_PL_DDR/ PG_2V5_PL_DDR	in	A38	NONE (UP)	+3.3V_STB	Power good pin for 1.5A low-dropout linear regulator with +2.5V output voltage (TPS74801DRC-U56)
PG+2V_MGT_PS/ PG_2V_MGT_PS	in	A1	NONE (UP)	+3.3V_STB	Power good pin for quad DC-DC microModule regulator with configurable 4A output array for +2.0V output voltage (LTM4644EY-U48)
PG+3.3V/ PG_3V3	in	A23	NONE (UP)	+3.3V_STB	Power good pin for quad DC-DC microModule regulator with configurable 4A output array with +3.3V output voltage (LTM4644EY-U1)
PWR_BTN	in	A12	UP (UP)	+3.3V_STB	Power button input (J40-Pin1)
PWR_STAT_GRN	out	B24	NONE (NONE)	+3.3V_STB	Red LED for power status display (D11-Red)
PWR_STAT_RED	out	A31	NONE (NONE)	+3.3V_STB	Green LED for power status display (D12-Green)
SRST_B	inout	B5	NONE (UP)	+1.8V	PS software reset (Active Low) (XCZU11EG-1FFVC1769I-U30S)
TCK	out	A5	NONE (NONE)	+1.8V	Zynq JTAG clock pin (XCZU11EG-1FFVC1760I-U30S)
TDI	out	B4	NONE (NONE)	+1.8V	Zynq JTAG data input pin (XCZU11EG-1FFVC1760I-U30S)
TDO	in	A6	NONE (NONE)	+1.8V	Zynq JTAG data output pin (XCZU11EG-1FFVC1760I-U30S)

THERM_N	in	A40	--- (UP)	+3.3V_STB	Overtemperature termal shutdown pin of temperature sensors (TMP461, U43, U47,U52,U57, U4) and temperature sensor with integrated fan control (LM96163-U61) /currently_not_used
TMS	out	A7	NONE (NONE)	+1.8V	Zynq JTAG mode select pin (XCZU11EG-1FFVC1760I-U30S)

Functional Description

JTAG

JTAG signals routed directly through the CPLD to FPGA. Access between CPLD and FPGA is multiplexed via JTAGEN pin of CPLD (B30) (logical one for CPLD, logical zero for FPGA).

CPLD JTAGEN (Dip switch S4-1)	Description
0	FPGA access
1	CPLD access

CPLD access

Boot Mode

TEB0912 supports JTAG, QSPI and SD card boot modes. Boot mode depends on the logic state of S2 dip switch pins that are connected with FPGA boot mode configuration pins.

S2-4	S2-3	S2-2	S2-1	Boot Mode
OFF	OFF	OFF	OFF	PS JTAG
OFF	OFF	ON	OFF	Quad-SPI (32b)
ON	ON	ON	OFF	SD1 LS (3.0)

Boot Mode table

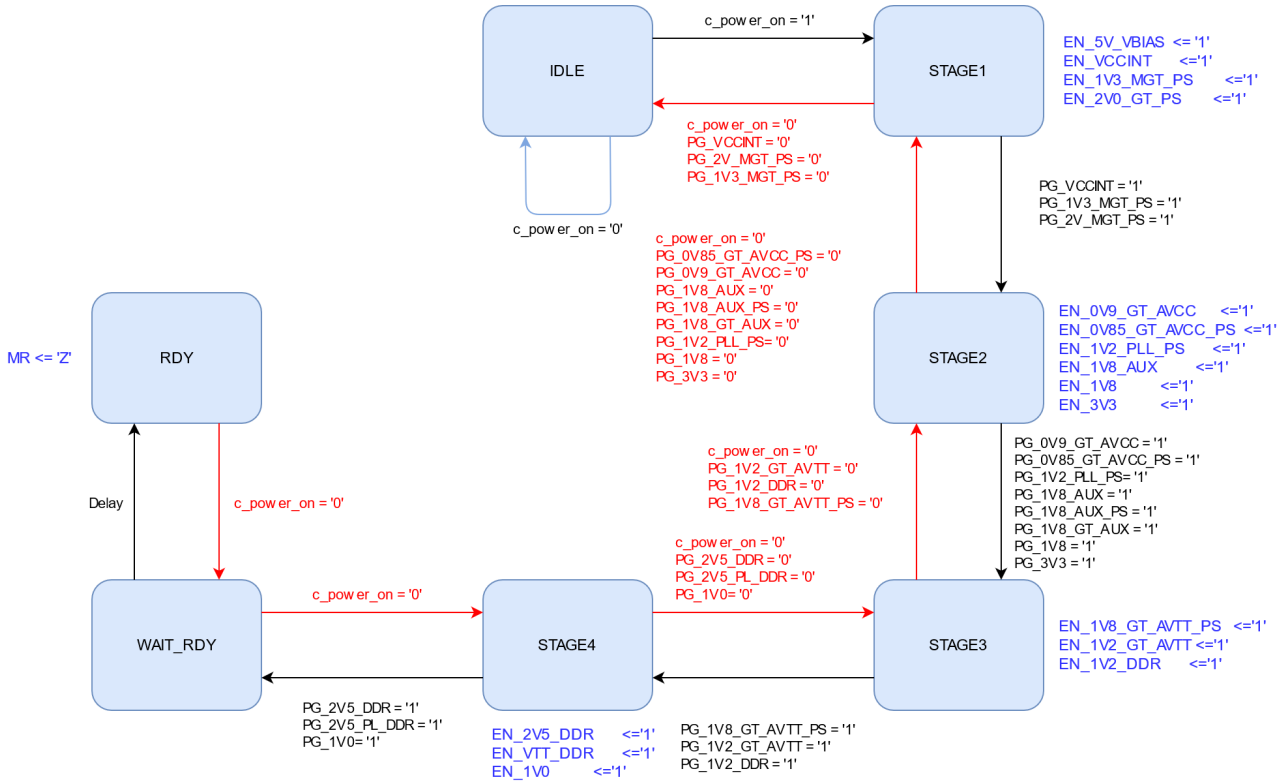
Power

In this board the CPLD is responsible for controlling and monitoring of output voltage and temperature of regulators and DC-DC converters. To control every converter chip or regualtor the CPLD monitors power good signal of regulators or DC-DC converters continuously to avoid over-voltage in the power system.

Enable Signal	Power Good Signal	Schematic Page	Input power Net	Regulator/ DC-DC Designator	Output power Net

EN+1.0V	PG+1.0V	PCIe_Switch_PWR	+1.37V	TPS74801DRC	U13	+1.0V
EN+2.5V_DDR	PG+2.5V_DDR PG+2.5V_PL_DDR	POWER3 POWER3	+3.3V +3.3V	TPS74801DRC TPS74801DRC	U55 U56	+2.5V_DDR +2.5V_PL_DDR
EN+1.8V	PG+1.8V	POWER3	+12V	LMT4644EY	U54	+1.8V
EN+1.2V_DDR	PG+1.2V_DDR	POWER3	+12V	LMT4644EY	U53	+1.2V_DDR
EN+1.8V_AUX	PG+1.8V_AUX PG+1.8V_GT_AUX PG+1.8V_AUX_PS	POWER2 POWER2 POWER2	+2V_MGT_PS +2V_MGT_PS +2V_MGT_PS	TPS74801DRC TPS74801DRC TPS74801DRC	U50 U49 U51	+1.8V_AUX +1.8V_GT_AUX +1.8V_AUX_PS
EN+1.2V_PLL_PS	PG+1.2V_PLL_PS	POWER1	+1.37V	TPS74801DRC	U46	+1.2V_PLL_PS
EN+0.85V_GT_AVCC_PS	PG+0.85V_GT_AVCC_PS	POWER1	+1.37V	TPS74801DRC	U45	+0.85V_GT_AVCC_PS
EN+1.8V_GT_AVTT_PS	PG+1.8V_GT_AVTT_PS	POWER3	+2V_MGT_PS	TPS74801DRC	U54	+1.8V_GT_AVTT_PS
EN+1.2V_GT_AVTT	PG+1.2V_GT_AVTT	POWER2	+12V	LTM4644EY	U48	+1.2V_GT_AVTT
EN+5V_BIAS	--	POWER6	+12V	ADP7102ACPZ-5.0-R7	U58	+5V_BIAS
EN+0.9V_GT_AVCC	PG+0.9V_GT_AVCC	POWER1	+12V	LTM4644EY	U44	+0.9V_GT_AVCC
EN+1.3V_MGT_PS	PG+1.3V_MGT_PS	POWER1	+12V	LTM4644EY	U44	+1.37V
EN+2V_MGT_PS	PG+2V_MGT_PS	POWER2	+12V	LTM4644EY	U48	+2V_MGT_PS
EN_VTT_DDR_PL EN_VTT_DDR_PS	--- ---	POWER4 POWER4	+3.3V +3.3V	TPS51206DSQ TPS51206DSQ	U2 U3	VTT_DDR_PL VTT_DDR_PS
EN+3.3V	PG+3.3V	POWER4	+12V	LTM4644EY	U1	+3.3V
EN_VCCINT	PG_VCCINT	POWER0	+12V	LTM4630EY	U42A	+0.85V_VCCINT

PG and EN Signals



Power Sequencing State Machine

Sequence	Power Net Name	Correspondent Regulator on Board	Enable Signal	PG Signal	Description

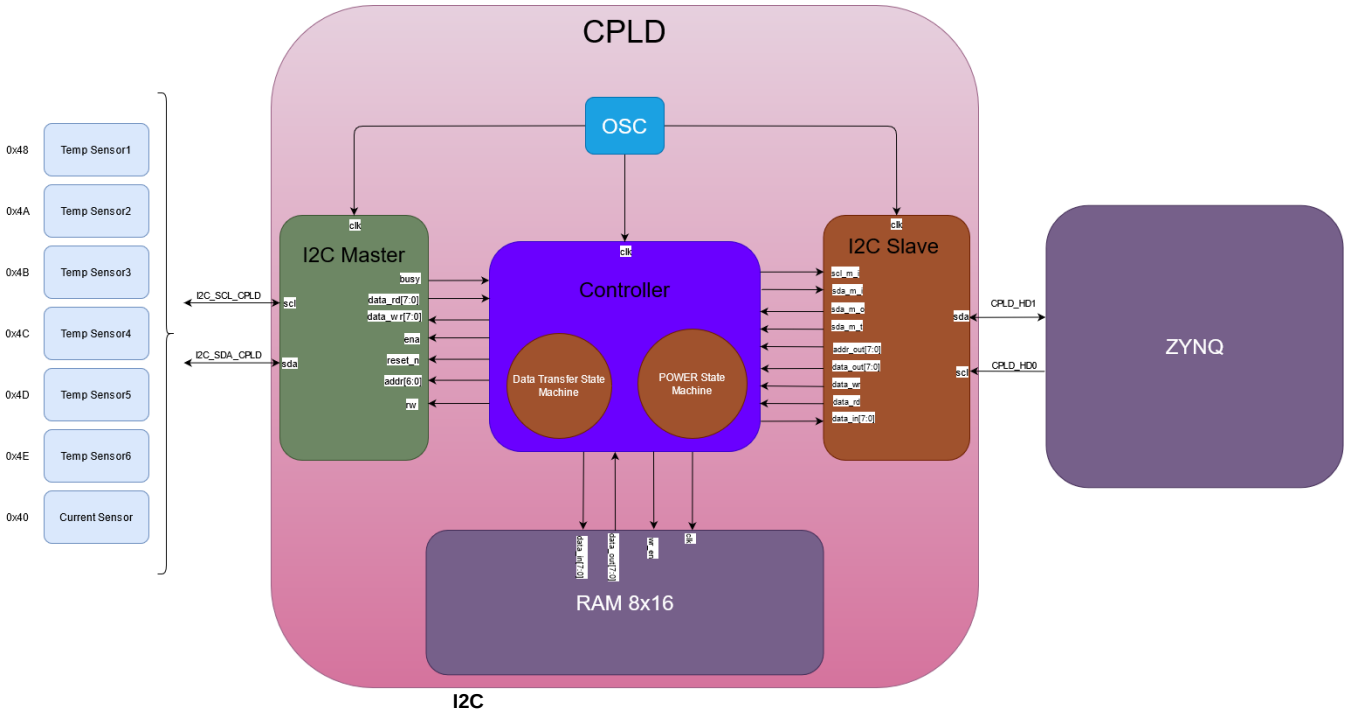
1	----- VCC_PSINTLP VCC_PSINTFP VCCINT ----- -----	+5V_BIAS +0. 85V_VCCINT +0. 85V_VCCINT +0. 85V_VCCINT +1.37V +2V_MGT_PS	U58 U42 U42 U42 U44 U48	EN_5V_VBIAS EN_VCCINT EN_VCCINT EN_VCCINT EN_1V3_GT_ PS EN_2V0_GT_ PS	---- PG_VCCINT PG_VCCINT PG_VCCINT PG_1V3_GT_ PS PG_2V_MGT _PS	• +5V_BIAS pin is connected to bias pin of +1.8V_GT_AUX , +1.8V_AUX , +1.8V_AUX_PS , +1.8V_GT_AVTT_PS , +0.85V_GT_AVCC_PS and +1.2V_PLL_PS regulator bias pins. • +1.37V pin is connected to regulator inputs for +0.85V_GT_AVCC_PS and +12V_PLL_PS voltages. • +2V_MGT_PS pin is connected to regulator inputs for +1.8V_AUX , +1.8V_GT_AUX , +1.8V_AUX_PS, +1.8V_GT_AVTT_PS voltages.

2	VCC_PSAUX VCC_PSADC VCCO_PSIO VCC_PSPLL VPS_MGTRA VCC VCC_PSDDR _PLL VCCINT_IO VCCBRAM VCCAUX VCCAUX_IO VMGTAVCC ----	+1. 8V_AUX_PS +1.8V +1.8V +1. 2V_PLL_PS +0. 85V_GT_AVC C_PS +1. 8V_AUX_PS +0. 85V_VCCINT +0. 85V_VCCINT +1.8V_AUX +1.8V_AUX +0. 9V_GT_AVCC +3.3V	U51 U53 U53 U46 U45 U51 U42 U42 U50 U50 U44 U1	EN_1V8_AUX EN_1V8 EN_1V8 EN_1V2_PLL _PS EN_0V85_GT _AVCC_PS EN_1V8_AUX EN_VCCINT EN_VCCINT EN_1V8_AUX EN_1V8_AUX EN_0V9_GT_ AVCC EN_3V3	PG_1V8_AUX PG_1V8 PG_1V8 PG_1V2_PLL _PS PG_0V85_GT _AVCC_PS PG_1V8_AUX PG_VCCINT PG_VCCINT PG_1V8_AUX PG_1V8_AUX PG_0V9_GT_ AVCC PG_3V3	• 3.3V pin is connected to DDR regulator inputs. (+2.5V_PL_DDR , +2.5V_DDR , VTT_DDR_PS and VTT_DDR_PL)
3	VPS_MGTRA VTT VCCO_PSDDR VMGTAVTT	+1. 8V_GT_AVTT _PS +1.2V_DDR +1. 2V_GT_AVTT	U54 U53 U48	EN_1V8_GT_ AVTT_PS EN_1V2_DDR EN_1V2_GT_ AVTT	PG_1V8_GT_ AVTT_PS PG_1V2_DDR PG_1V2_GT_ AVTT	• +1.2V_DDR is connected to DDR_PL and DDR_PS regulator inputs.
4	---- ---- ----	VTT_DDR_PL , VTT_DDR_P S +2. 5V_PL_DDR , +2.5V_DDR +1.0V	U2,U3 U55,U56 U13	EN_VTT_DDR EN_2V5_DDR EN_1V0	---- PG_2V5_DD R , PG_2V5_PL_ DDR PG_1V0	• +1.0V is for PCIe switch.

Power sequencing table

I2C

The main interface in the system is I2C interface. The user can input the data in the system through i2c slave subsystem. The entered data is stored in RAM memory. The state machine reads the stored data and communicates with corresponding sensor through i2c master subsystem and stores the feedback data again in RAM memory. The user can read back reported data for example temperature value.



I2C

Internal Registers

Ram memory is a 16x8 Byte Memory.

Register Name	Register address	Bits	CPLD	FPGA
config_reg	0x00	7 6 5 4 3 2 1 0 0 0 0 0 0 read_bit write_bit start_bit	Read	Write
sensor_addr	0x01	8-bits	Read	Write
pointer_reg_byte	0x02	8-bits	Read	Write
data_to_write	0x03	8-bits	Read	Write
Reserved	0x04	8-bits		
Reserved	0x05	8-bits		
Reserved	0x06	8-bits		
Reserved	0x07	8-bits		
state register	0x08	7 6 5 4 3 2 1 0 0 0 0 0 0 0 0 data_trans_busy	Write	Read

data_to_read	0x09	8-bits	Write	Read
Reserved	0x0A	8-bits		
Reserved	0x0B	8-bits		
Reserved	0x0C	8-bits		
Reserved	0x0D	8-bits		
Reserved	0x0E	8-bits		
Reserved	0x0F	8-bits		

Registers

The memory consists of the following registers:

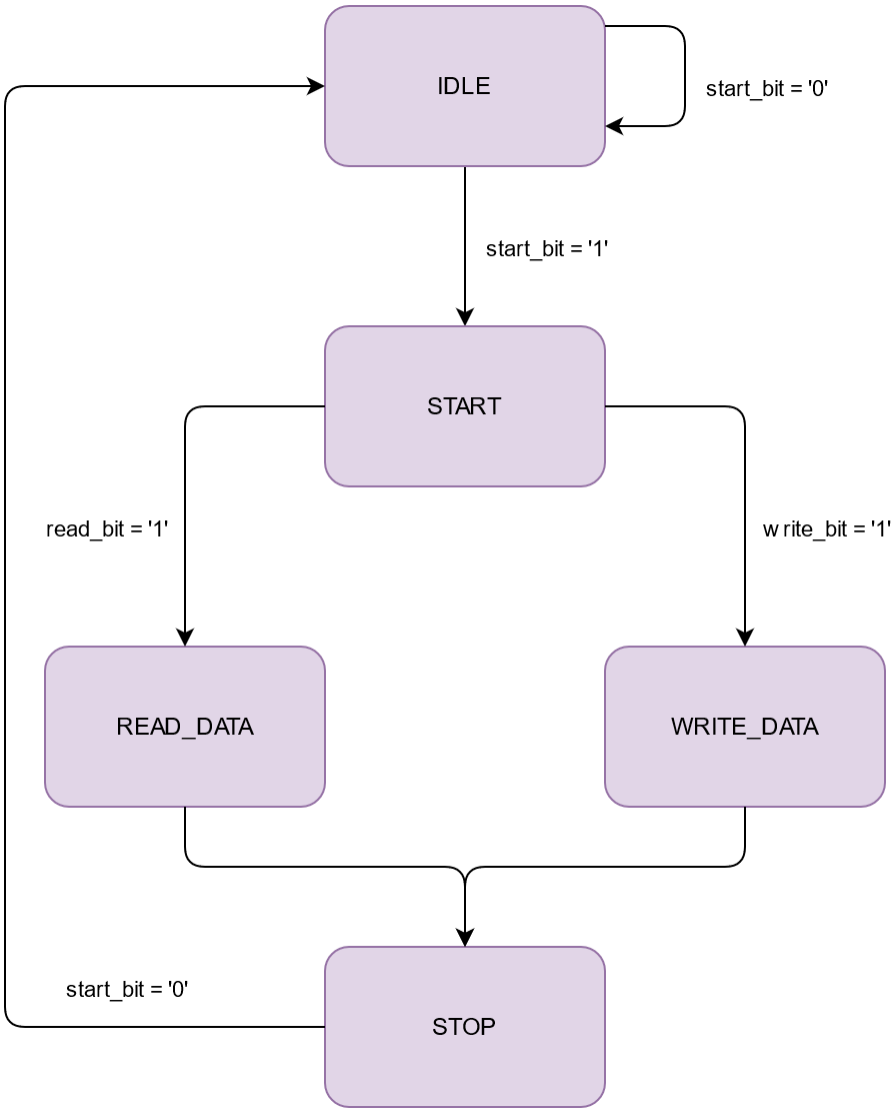
- config_reg
- sensor_addr
- pointer_reg_byte
- data_to_write
- state_reg
- data_to_read

Sensor_addr register consists of sensor address that the temperature should be read from. Pointer_reg_byte is sensor internal register address that is to be written to or read from. Data_to_write register consists of data that in pointer_reg_byte will be written. The readed data from sensor is saved in data_to_read register. As long as state machine is busy , it will be state_teg value equal to 0x01. Config_reg consists of control bits. To start data transfer in state machine start_bit must be set to 1. If write_bit set to one, the inhalt of data_to_write will be written in pointer_reg_byte register of sensor . To read the inhalt of pointer_reg_byte register of sensor the read_bit must be set to 1.

Transfer state machine

To manage data transfer between RAM memory and i2c master subsystem that is connected with sensors, it is necessary to design a state machine. This state machine will be controlled with control bits of config_reg register. If start_bit is activated, state machine begins to transfer data between RAM memory and i2c master subsystem. If write_bit is set to one, saved data in RAM memory will be written in temperature sensor. If read_bit is set to one, temperature value will be readed from sensor and will be saved in RAM memory. Every state in the state machine consists of a state machine to manage i2c master communications.

In the following diagram this state machine construction is shown:



Data Transfer State Machine

Sensors on board

Sensor Name	Sensor I2C address	connection	Description	Chip Name	Description
+12V, Current sensor	0x40	CPLD	Currently not suppported	INA219	For more information refer to Datasheet
Temperature sensor of +0. 85V_VCCINT DC-DC	0x48	CPLD	Supported	TMP461	For more information refer to Datasheet
Temperature sensor of DDR power and +1.8V	0x4A	CPLD	Supported	TMP461	---

Temperature sensor of +3.3V	0x4B	CPLD	Supported	TMP461	---
Temperature sensor with integrated fan controller	0x4C	CPLD	Supported	TMP461	---
Temperature sensor of +1. 2V_GT_AVTT	0x4D	CPLD	Supported	TMP461	---
Temperature sensor of +0. 9V_GT_AVCC	0x4E	CPLD	Supported	TMP461	---

Sensors

All temperature sensors are TMP461 of texas instruments. When this sensor is in shutdown mode, a single conversion is started by writing any value in one_shot_start register (poniter address 0x0F). The device returns to shutdown mode when the conversion and cycle completes. The result value is saved in high and low byte of Local/ Remote temperature registers. The high byte consists of temperature integer value and low byte consists of fraction part of temperature value. (Pointer addresses 0x00,0x15 for local temperature register and pointer addresses 0x01,0x10 for remote temperature register). The channel enable register (read address 16h, write address 16h) enables or disables the temperature conversion of remote and local temperature sensors. LEN (bit 0) of the channel enable register enables/disables the conversion of local temperature. REN (bit 1) of the channel enable register enables/disables the conversion of remote temperature. Both LEN and REN are set to 1 (default), this enables the ADC to convert both local and remote temperatures.

The TMP461 device is a digital temperature sensor that combines a local temperature measurement channel and a remote-junction temperature measurement channel in a single WQFN-10 package. The device is two-wire and SMBus-interface-compatible with nine pin-programmable bus address options, and is specified over a temperature range of –40°C to 125°C. The TMP461 device also contains multiple registers for programming and holding configuration settings, temperature limits, and temperature measurement results. In the following it is listed important registers of this sensor:

- STATUS REG----------Addr ---> 0x02 (read only) (Default N/A)
- Local temperature register MSB 8 bits---------Addr ---> 0x00 (read only) (Default 0x00)
- Local temperature register LSB 4 bits----------Addr ---> 0x15 (read only) (Default 0x00)
- Remote temperature register MSB 8 bits------Addr ---> 0x01 (read only) (Default 0x00)
- Remote temperature register LSB 4 bits-------Addr ---> 0x10 (read only) (Default 0x00)
- Configuration register----------Addr ---> 0x03 (read/write) (Default 0x00)
- Channel enable register----------Addr ---> 0x16 (read/write) (Default 0x03)
- Conversion rate register----------Addr ---> 0x04 (read/write) (Default 0x08)
- One-shot start register----------Addr ---> 0x0F (read/write) (Default N/A)

The INA219 is a high-side current shunt and power monitor with an I2C interface. The INA219 monitors both shunt drop and supply voltage, with programmable conversion times and filtering. A programmable calibration value, combines with an internal multiplier, enables direct readouts in amperes. An additional multiplying register calculates power in watts. The I2C interface features 16 programmable accesses.

To access these sensors through ZynqMP can be executed the following instructions in linux console consecutively:

1. Write device address
   - `i2cset -y 2 0x20 0x01 <sensor address>  --> This command writes sensor address in RAM memory address 0x01 (sensor_addr register)`
2. Write register address
   - `i2cset -y 2 0x20 0x02 <register address>  --> This command writes desired register address in RAM memory address 0x02 (pointer_reg_byte register)`
3. Write data that should be written in the register

- `i2cset -y 2 0x20 0x03 <data to write>` --> This command writes desired value in RAM memory address 0x03 (data_to_write register)

4. Start to write data
   - `i2cset -y 2 0x20 0x00 0x03` --> This command set write_bit to one. (Write command)
5. Stop writing data
   - `i2cset -y 2 0x20 0x00 0x00` --> This command stops writing in RAM memory.
6. Start to read data
   - `i2cset -y 2 0x20 0x00 0x05` --> This command set read_bit to one. (Read command)
7. Stop reading data
   - `i2cset -y 2 0x20 0x00 0x00` --> This command stops reading from RAM memory.
8. Read data_to_read register
   - `i2cget -y 2 0x20 <data to read>` --> This command reads data from desired register.

For example to read a temperature sensor it is necessary to give the following commands in linux console:

- `i2cset -y 2 0x20 0x01 <sensor address>` --> Writing device address
- `i2cset -y 2 0x20 0x02 0x0F` --> Writing One-shot register address
- `i2cset -y 2 0x20 0x03 0xFF` --> Writing any value in the register to start converting of ADC in sensor
- `i2cset -y 2 0x20 0x00 0x03` --> Start to write these values
- `i2cset -y 2 0x20 0x00 0x00` --> To turn i2c master data transfer off
- `i2cset -y 2 0x20 0x02 0x00` --> Writing address of local temperature high byte register that consists of the temperature value
- `i2cset -y 2 0x20 0x00 0x03` --> Start to write these values
- `i2cset -y 2 0x20 0x00 0x00` --> To turn i2c master data transfer off
- `i2cset -y 2 0x20 0x00 0x05` --> Start to read temperature value of sensor and save it in data_to_read register
- `i2cset -y 2 0x20 0x00 0x00` --> To turn i2c master data transfer off
- `i2cget -y 2 0x20 0x09` --> Reading temperature value from data_to_read register
- `i2cset -y 2 0x20 0x02 0x15` --> Writing address of local temperature low byte register that consists of fraction of the temperature value
- `i2cset -y 2 0x20 0x00 0x03` --> Start to write these values
- `i2cset -y 2 0x20 0x00 0x00` --> To turn i2c master data transfer off
- `i2cset -y 2 0x20 0x00 0x05` --> Start to read temperature value of sensor and save it in data_to_read register

- `i2cset -y 2 0x20 0x00 0x00 --> To turn i2c master data transfer off`
- `i2cget -y 2 0x20 0x09 --> Reading temperature fraction value from data_to_read register`

If the following shell script is executed in linux console it can be read all temperatures of all temperature sensors on the board. This script file will be executed automatically while booting, if this file is copied to SD card.

init.sh

```
#!/bin/sh

set sensor_addr=0                       # Temperature = Temp+Fraction*16^-
1 °C for example 50+1*16^-1 = 50.0625 °C
Temp=0                                  # 8bits
Fraction=0                              #
4bits
i=0
n1=0
n2=0
for sensor_addr in 0x48 0x4A 0x4B 0x4C 0x4D 0x4E
do
        echo "Sensor Address $sensor_addr:"
        echo "Reading Sensor $i:"
        i2cset -y 2 0x20 0x01 $sensor_addr          # Write sensor address
in RAM memory address 0x01
        i2cset -y 2 0x20 0x02 0x0F                  # Write one-shot-start
register address in 0x02 of RAM
        i2cset -y 2 0x20 0x03 0xFF                  # Write 0xFF value in
0x03 address of RAM
        i2cset -y 2 0x20 0x00 0x03                  # Writing in sensor
        i2cset -y 2 0x20 0x00 0x00                  # Stop writing
        i2cset -y 2 0x20 0x02 0x00                  # Write 0x00 value
(local temperature register high byte address) in 0x02 of RAM memory
        i2cset -y 2 0x20 0x00 0x03                  # Writing in sensor
        i2cset -y 2 0x20 0x00 0x00                  # Stop writing
        i2cset -y 2 0x20 0x00 0x05                  # Reading sensor
        i2cset -y 2 0x20 0x00 0x00                  # Stop reading
        Temp=`i2cget -y 2 0x20 0x09`                # Read temperature
value stored in 0x09 address of RAM memory
        #echo $Temp
        n1=$(($Temp))
        #echo $n1
        i2cset -y 2 0x20 0x02 0x15                  # Write 0x15 value
(local temperature register low byte address) in 0x02 of RAM memory
        i2cset -y 2 0x20 0x00 0x03                  # Writing in sensor
        i2cset -y 2 0x20 0x00 0x00                  # Stop writing
        i2cset -y 2 0x20 0x00 0x05                  # Reading sensor
        i2cset -y 2 0x20 0x00 0x00                  # Stop reading
        Fraction=`i2cget -y 2 0x20 0x09`            # Read temperature
value stored in 0x09 address of RAM memory
        #echo $Fraction
        n2=$((Fraction>>4))                         # Shift bits 4
times
        #echo $n2
        echo "-----------------------------"
        #printf "Sensor %d Temperature = %d Celsius \n" $i $Temp
        #printf "Sensor %d Fraction = %d \n" $i $Fraction
        echo "Sensor $i Temperature = "
        awk "BEGIN {print  $n1+$n2*16**-1}"
        echo "Celsius"
        echo "-----------------------------"
        let i++
done
```

```
Init Start
Run init.sh from SD card
Sensor Address 0x48:
Reading Sensor 0:
------------------------------
Sensor 0 Temperature =
55.5625
Celsius
------------------------------
Sensor Address 0x4A:
Reading Sensor 1:
------------------------------
Sensor 1 Temperature =
56.125
Celsius
------------------------------
Sensor Address 0x4B:
Reading Sensor 2:
------------------------------
Sensor 2 Temperature =
58.3125
Celsius
------------------------------
Sensor Address 0x4C:
Reading Sensor 3:
------------------------------
Sensor 3 Temperature =
46
Celsius
------------------------------
Sensor Address 0x4D:
Reading Sensor 4:
------------------------------
Sensor 4 Temperature =
55.875
Celsius
------------------------------
Sensor Address 0x4E:
Reading Sensor 5:
------------------------------
Sensor 5 Temperature =
57.125
Celsius
------------------------------
Init End
Starting syslogd/klogd: done
Starting tcf-agent: OK

PetaLinux 2020.2 petalinux ttyPS0

petalinux login: root
Password:
root@petalinux:~#
```

LED

Green LED

State	Blink sequence	Comment
IDLE	OFF	Power sequencing can not be started. Power button is not pushed or is not pushed correctly.
STAGE1	ooooooo*	The following power good signals are faulty. PG_VCCINT PG_1V3_MGT_PS PG_2V_MGT_PS
STAGE2	oooooo**	The following power good signals are faulty. The error may be due to a problem in a corresponding DC-DC converter or regulator. PG_0V9_GT_AVCC PG_0V85_GT_AVCC_PS PG_1V2_PLL_PS PG_1V8 PG_3V3 PG_1V8_AUX PG_1V8_AUX_PS PG_1V8_GT_AUX
STAGE3	ooooo***	The following power good signals are faulty. The error may be due to a problem in a corresponding DC-DC converter or regulator. PG_1V2_DDR PG_1V8_GT_AVTT_PS PG_1V2_GT_AVTT
STAGE4	oooo****	The following Power good signals are faulty.The error may be due to a problem in a corresponding DC-DC converter or regulator. PG_2V5_DDR PG_2V5_PL_DDR PG_1V0
WAIT_RDY	********	The state machine remains in this stage as soon as a counter is not overflowed. After overflowing the counter the state machine will jump in the next stage.
RDY	ON	Power is ok and the FPGA is configured successfully.

Green LED States

RED LED

Status	Blink sequence	Comment

pg_all = '0'	********	One of the power good signals are faulty. The error may be due to a problem in a DC-DC converter or regulator.
MR = '0'	*****ooo	Reset button is pushed.
SRST_B ='0'	****oooo	PS software reset (Active Low) is activated.
FPGA_DONE ='0'	***ooooo	FPGA PL is not configured.
FPGA_DONE ='0'	**oooooo	FPGA PL is not configured.
FTDI_PWR_EN_N='1'	*ooooooo	FTDI chip USB SUSPEND mode or device has not been co nfigured.
else	OFF	

Red LED States

Appx. A: Change History and Legal Notices

Revision Changes

- Changes REV02 to REV03:
  - Added i2c slave to communicate with FPGA
  - Added i2c master to read and write temperature sensors value
  - Added i2c master state machine to manage communication between CPLD and temp. sensors
  - Added a 8x16 byte RAM to save data in RAM
  - Correction of power sequencing
- Changes REV01 to REV02:
  - Power Management
  - FAN enable
  - LED blink sequencing
- Changes REV00 to REV01:
  - Power on (min)
  - UART
  - JTAG

Document Change History

To get content of older revision got to "Change History" of this page and select older document revision number.

Date	Document Revision	CPLD Firmware Revision	Supported PCB Revision	Authors	Description
Error re Ambigu	Error rendering macro 'page-info' Ambigu	REV03 Error rendering macro 'page-info' Ambigu	REV02, REV03	Error rendering macro 'page-info' Ambigu	• REV03 release • Firmware release (SC-PCM-TEB0912-0302_SC0912-03_20210622.zip)

2021-02-16	v.39	REV02	REV02, REV03	Mohsen Chamanbaz	• REV02 release • Firmware release (SC-PGM-TEB0912-02_SC0912-02_20191127.zip)
	All			**Error rendering macro 'page-info'** Ambiguous method overloading for method jdk.proxy279.$Proxy4022#hasContentLevell	

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Error rendering macro 'page-info'

Ambiguous method overloading for method jdk.proxy279.$Proxy4022#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]