

TE0300 B2B Connectors Pin Descriptions

The following tables reports pin-out information of B2B (board-to-board) receptacle connectors J4 and J5 respectively. The reference design summaries report the resources needed by the reference design on TE0300 modules of different dimensions (1200 and 1600 versions).

TE0303 Prototyping Carrier Board connection with TE0300 module

The connection between TE0300 module connectors J(M)4/J(M)5 and TE0303 Prototyping Carrier Board connectors J1/J2/J3/J4 is documented [here](#). TE0300 modules and TE0630 modules fit onto the same TE0303 Prototyping Carrier Board.

TE0304 Application Demo Carrier Board connections with TE0300 module

The connection between TE0300 module connectors J(M)4/J(M)5 and TE0304 Application Demo Carrier Board connectors J1/J2/J3/J4 is documented [here](#). TE0300 modules and TE0630 modules fit onto the same TE0304 Application Demo Carrier Board.

B2B Connector Pin-Outs

Connector J4: Pin-Out Information

pin	B2Bname	FPGApin	FPGAname	bank	dir	supply	diff	diff	supply	dir	bank	FPGAname	FPGApin	B2Bname	pin
1	VccIO	-	VccO	0	I	-	-	-	-	I	0	VccO		VccIO	2
3	VccIO	-	VccO	0	I	-	-	-	-	I	0	VccO	-	VccIO	4
5	B3_L01_P	C1	IO_L01P	3	IO	3.3 V	Y	Y	3.3 V	IO	3	IO_L07P	G6	B3_L07_P	6
7	B3_L01_N	C2	IO_L01N	3	IO	3.3 V	Y	Y	3.3 V	IO	3	IO_L07N	G5	B3_L07_N	8
9	B3_L02_P	D1	IO_L02P	3	IO	3.3 V	Y	Y	3.3 V	IO	3	IO_L03N	E1	B3_L03_N	10
11	B3_L02_N	D2	IO_L02N/ VREF	3	IO	3.3 V	Y	Y	3.3 V	IO	3	IO_L03P	E2	B3_L03_P	12
13	GND													GND	14
15	B0_IO_C3	C3	IO_L25P	0	IO	VccIO	N	Y	VccIO	IO	0	IO_L19_P	F7	B0_L19_P	16
17	B0_L24_N	B4	IO_L24_N	0	IO	VccIO	Y	Y	VccIO	IO	0	IO_L19N/ VREF	E7	B0_L19_N	18
19	B0_L24_P	A4	IO_L24P	0	IO	VccIO	Y	Y	VccIO	IO	0	IO_L21N	E6	B0_L21_N	20
21	B0_IO_C4	C4	IO	0	IO	VccIO	N	Y	VccIO	IO	0	IO_L21P	D6	B0_L21_P	22
23	GND													GND	24
25	B0_L23_N	D5	IO_L23N/ VREF	0	IO	VccIO	Y	Y	VccIO	IO	0	IO_L18N/ VREF	D7	B0_L18_N	26
27	B0_L23_P	C5	IO_L23P	0	IO	VccIO	Y	Y	VccIO	IO	0	IO_L18P	C7	B0_L18_P	28
29	B0_L20_P	B6	IO_L20P	0	IO	VccIO	Y	Y	VccIO	IO	0	IO_L17N	F8	B0_L17_N	30
31	B0_L20_N	A6	IO_L20N	0	IO	VccIO	Y	Y	VccIO	IO	0	IO_L17P	E8	B0_L17_P	32
33	3.3 V													3.3 V	34
35	B0_IO_A7	A7	IO	0	IO	VccIO	N	N	VccIO	IO	0	IO	A8	B0_IO_A8	36
37	B0_IO_G9	G9	IO	0	IO	VccIO	N	Y	VccIO	IO	0	IO_L14N/ GCLK11	D9	GCLK_L14_N	38
39	GCLK_L13_P	B8	IP_L13P/ GCLK8	0	I	VccIO	Y	Y	VccIO	IO	0	IO_L14P/ GCLK10	C9	GCLK_L14_P	40
41	GCLK_L13_N	B9	IP_L13N/ GCLK9	0	I	VccIO	Y	Y	VccIO	IO	0	IO_L11N/ GCLK5	E10	GCLK_L11_N	42
43	GND							Y	VccIO	IO	0	IO_L11P/ GCLK4	D10	GCLK_L11_P	44
45	GCLK_L12_P	B10	IO_L12P/ GCLK6	0	IO	VccIO	Y							GND	46
47	GCLK_L12_N	A10	IO_L12N/ GCLK7	0	IO	VccIO	Y	Y	VccIO	IO	0	IO_L09N	D11	B0_L09_N	48
49	B0_L15_P	E9	IO_L15P	0	IO	VccIO	Y	Y	VccIO	IO	0	IO_L09P	C11	B0_L09_P	50
51	B0_L15_N	F9	IO_L15N	0	IO	VccIO	Y	N	VccIO	IO	0	IO	A11	B0_IO_A11	52
53	2.5 V													2.5 V	54
55	B0_L08_P	E11	IO_L08P	0	IO	VccIO	Y	N	VccIO	IO	0	IO/VREF	B11	B0_IO_B11	56
57	B0_L08_N	F11	IO_L08N	0	IO	VccIO	Y	N	VccIO	IO	0	IO	A12	B0_IO_A12	58
59	B0_L05_P	A13	IO_L05P	0	IO	VccIO	Y	Y	VccIO	IO	0	IO_L06P	F12	B0_L06_P	60
61	B0_L05_N	B13	IO_L05N/ VREF	0	IO	VccIO	Y	Y	VccIO	IO	0	IO_L06N	E12	B0_L06_N	62
63	GND													GND	64
65	B0_L04_N	A14	IO_L04N	0	IO	VccIO	Y	N	VccIO	IO	0	IO	D13	B0_IO_D13	66
67	B0_L04_P	B14	IO_L04P	0	IO	VccIO	Y	N	VccIO	IO	0	IO	E13	B0_IO_E13	68
69	B0_L03_N	C14	IO_L03N/ VREF	0	IO	VccIO	Y		3.3 V	I	2	TDI	A2	TDI	70
71	B0_L03_P	D14	IO_L03P	0	IO	VccIO	Y		3.3 V	O	2	TDO	C16	TDO	72
73	1.2 V													1.2 V	74
75	B0_L01_N	A16	IO_L01N	0	IO	VccIO	Y		3.3 V	I	2	TCK	A17	TCK	76
77	B0_L01_P	B16	IO_L01P	0	IO	VccIO	Y		3.3 V	I	2	TMS	D15	TMS	78
79	GND													GND	80

Connector J5: Pin-Out Information

pin	B2Bname	FPGApin	FPGAname	bank	dir	supply	diff	diff	supply	dir	bank	FPGAname	FPGApin	B2Bname	pin
1	5Vb2b				I					I				5Vb2b	2
3	5Vb2b				I					I				5Vb2b	4
5	5V				O					I				/MR	6
7	B2B_D_P / USB				IO		Y			O				/RESET	8

9	B2B_D_N / USB					IO		Y				O				RESET	10
11	GND															GND	12
13	B3_L22_P	P3	IO_L22P	3		IO	3.3 V	Y	N	3.3 V	IO	3	IO_L24P	T2		B3_IO_T2	14
15	B3_L22_N	P4	IO_L22N	3		IO	3.3 V	Y	Y	3.3 V	IO	3	IO_L21N	P1		B3_L21_N	16
17	B2_IP_V4	V4	IP_L02P	2		I	3.3 V	N	Y	3.3 V	IO	3	IO_L21P	P2		B3_L21_P	18
19	B3_L20_P	N4	IO_L20P	3		IO	3.3 V	Y	Y	3.3 V	IO	3	IO_L23N	R2		B3_L23_N	20
21	B3_L20_N	N5	IO_L20N	3		IO	3.3 V	Y	Y	3.3 V	IO	3	IO_L23P	R3		B3_L23_P	22
23	GND															GND	24
25	B2_L04_N	T5	IO_L04N	2		IO	3.3 V	Y	N	3.3 V	IO	3	IO_L18N	M3		B3_IO_L18N	26
27	B2_L04_P	R5	IO_L04P	2		IO	3.3 V	Y	N	3.3 V	IO	2	IO_L03P/ DOUT /BUSY	U4		B2_IO_L03	28
29	B2_L05_P	R6	IO_L05P	2		IO	3.3 V	Y	N	3.3 V	IO	2	IO/ VREF	U5		B2_IO_U5	30
31	B2_L05_N	P6	IO_L05N	2		IO	3.3 V	Y	Y	3.3 V	IO	2	IO_L06P	V5		B2_L06_P	32
33	B2_IO_V7	V7	IO	2		IO	3.3 V	N	Y	3.3 V	IO	2	IO_L06N/ VREF	V6		B2_L06_N	34
35	3.3 V															3.3 V	36
37	B2_L07_N	P7	IO_L07N	2		IO	3.3 V	Y	N	3.3 V	IO	2	IO	U6		B2_IO_U6	38
39	B2_L07_P	N7	IO_L07P	2		IO	3.3 V	Y	Y	3.3 V	IO	3	IO_L17N/ VREF	L5		B3_L17_N	40
41	B2_GCLK12	M9	IO_L12N/ D6 /GCLK12	2		I	3.3 V	N	Y	3.3 V	IO	3	IO_L17P	L6		B3_L17_P	42
43	GND															GND	44
45	B2_L10_N	T8	IO_L10N	2		IO	3.3 V	Y	N	3.3 V	I	2	IP_L08P	T7		B2_IP_T7	46
47	B2_L10_P	R8	IO_L10P	2		IO	3.3 V	Y	N	3.3 V	I	2	IP_L11P	U8		B2_IP_U8	48
49	B2_GCLK_L13_N	V9	IO_L13N/ D3 /GCLK15	2		IO	3.3 V	Y	Y	3.3 V	IO	3	IO_L19P	M5		B3_L19_P	50
51	B2_GCLK_L13_P	U9	IO_L13P/ D4 /GCLK14	2		IO	3.3 V	Y	Y	3.3 V	IO	3	IO_L19N	M6		B3_L19_N	52
53	2.5 V						3.3 V									2.5 V	54
55	B2_L18_N	N11	IO_L18N	2		IO	3.3 V	Y	Y	3.3 V	IO	2	IO_L09P	P8		B2_L09_P	56
57	B2_L18_P	P11	IO_L18P	2		IO	3.3 V	Y	Y	3.3 V	IO	2	IO_L09N	N8		B2_L09_N	58
59	B2_L20_N	R12	IO_L20N	2		IO	3.3 V	Y	N	3.3 V	IO	2	IO	P9		B2_IO_P9	60
61	B2_L20_P	T12	IO_L20P	2		IO	3.3 V	Y	N	3.3 V	IO	2	IO	R11		B2_IO_R11	62
63	GND															GND	64
65	B2_L19_N	V13	IO_L19N/ VREF	2		IO	3.3 V	Y	N	3.3 V	IO	2	IO_L15N/ D1 /GCLK3	P10		B2_IO_P10	66
67	B2_L19_P	V12	IO_L19P	2		IO	3.3 V	Y	N	3.3 V	IO	2	IO/ D5	R9		B2_IO_R9	68
69	B2_L22_N	R13	IO_L22N/ A22	2		IO	3.3 V	Y	Y	3.3 V	IO	2	IO_L21N	P12		B2_L21_N	70
71	B2_L22_P	P13	IO_L22P/ A23	2		IO	3.3 V	Y	Y	3.3 V	IO	2	IO_L21P	N12		B2_L21_P	72
73	1.2 V															1.2 V	74
75	B2_L24_P	T14	IO_L24P/ A21	2		IO	3.3 V	Y	N	3.3 V	I	2	IP_L23P	V14		B2_IP_V14	76
77	B2_L24_N	R14	IO_L24N/ A20	2		IO	3.3 V	Y	N	3.3 V	IO	2	IO	U13		B2_IO_U13	78
79	GND															GND	80