TE0300 USB Interface

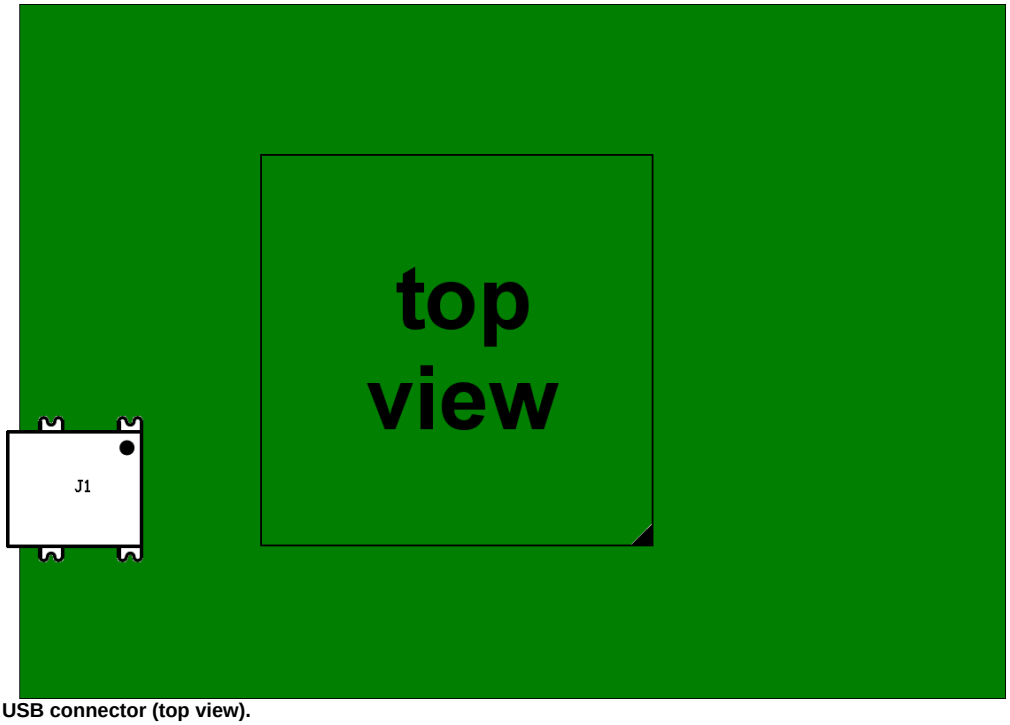
USB communication can be performed in one of the following two ways:

- through a USB connector
- through USB lines at one B2B connector.

> ⚠ Only one connection type at one time is allowed.

USB Connector

TE0300 is provided with a USB mini-B receptacle (device) connector J1 on the top side.



USB connector (top view).

USB mini-B receptacle (device) connector.

The USB cable provides for

- Power supply.

- Configuration by means of the Firmware Upgrade Tool (FUT), recommended for field upgrades. Please use a dedicated JTAG Adapter during development.
- Data communication channel during operation.

USB Pins

USB communication can be performed over 2 pins of B2B connector J5 as detailed in the table below. Ensure resistors R4 and R3 are populated to connect USB B2B pins B2B_D_P and B2B_D_P to USB lines D_P and D_P respectively.

pin number	pin name	signal name	description
7	B2B_D_P	D_P	USB data + (D+)
9	B2B_D_N	D_N	USB data - (D-)

USB pins at B2B connector J5.

TE0300 USB Controller

TE0300 is equipped with a Cypress EZ-USB FX2 controller to provide a high-speed USB 2.0 interface. The controller uses 4 interfaces (see here):

- USB interface (to USB connector);
- I^2C interface (to EEPROM);
- SPI interface (to FPGA and Flash);
- FIFO interface (to FPGA).

The I^2C interface connects the USB controller to the EEPROM chip, which stores vendor ID and device ID. See chapter DIP Switch for available options.
The SPI interface id used to communicate with the FPGA and to access the SPI serial Flash chip.
The FIFO interface provides a high-speed communication channel with the FPGA. The interface can transfer up to 48 MB/s burst rate.