TE0300 Clock Networks

24 MHz Clock Oscillator

The module has a 24 MHz SMD clock oscillator providing a clock source for both the USB microcontroller and the FPGA as detailed in the table below.

Signal	FPGA pin	FPGA ball
24MHZ1	IO_L12P_2(bank 2)	N9

24 MHz clock signal details.

Digital Clock Manager (DCM)

The DCMs of the FPGA can be used to synthesize arbitrary clock frequencies from any on-board clock network, differential clock input pair or single-ended clock input. For further reference, please read Xilinx DS485:Digital Clock Manager (DCM) Module and the DCM chapter in Xilinx UG331: Spartan-3 Generation FPGA User Guide.

Interface Clock (IFCLK)

The IFCLK line synchronizes the communication between the EZ-USB FX2LP USB FX2 microcontroller and the FPGA as detailed in the table below.

signal	FPGA pin	FPGA ball	FPGA bank
IFCLK	LHCLK5(bank 3)	K4	3

Interface clock (IFCLK) signal details.

Main Clock Oscillator

The module has a main SMD clock oscillator providing a clock source for the FPGA as detailed in the table below.

signal	FPGA pin	FPGA ball	FPGA bank
100MHZ125MHZ	GCLK0(bank 2)	U10	2

Main clock signal details.

Standard frequencies are 100 MHz and 125 MHz (please visit Trenz Electronic website for current ordering information). The lower the main clock frequency, the lower the module power consumption. Moreover, as the main clock is preferably used as DDR SDRAM clock, a lower clock frequency makes easier for the development tools to meet the timing requirements (particularly for DDR SDRAM). For customized boards, this clock can be changed according to user requirements.